

FAULT DIAGNOSIS OF H. V. D. C. CONVERTERS USING MICROPROCESSOR

**A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of**

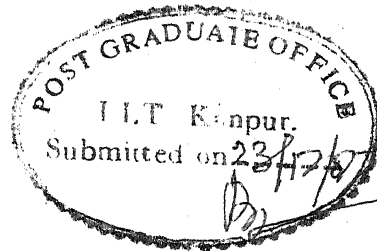
MASTER OF TECHNOLOGY

**by
P. VARAN KUMAR REDDY**

to the

**DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR**

DECEMBER, 1987



CERTIFICATE

This is to certify that the thesis entitled 'FAULT DIAGNOSIS OF H.V.D.C. CONVERTERS USING MICROPROCESSOR' submitted by P. Varan Kumar Reddy in partial fulfilment of the requirements for the Degree of Master of Technology has been carried out under my supervision and this has not been submitted elsewhere for a degree.

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- P. Varan Kumar Reddy

ABSTRACT

This thesis deals with fault diagnosis scheme for H.V.D.C. converters. This scheme makes use of information regarding firing pulse instants, the three a.c. line voltages and ON/OFF state of valves for which necessary hardware is developed. The necessary software has been developed for fault diagnosis to interface the hardware with workstation.

Fault diagnosis scheme presented here is capable of detecting various faults which commonly occur in a H.V.D.C. converter, viz., misfire and single commutation failure of a valve. The testing is done by simulating the faults in the scaled down model of H.V.D.C. simulator. Workstation which was used to do processing also consists of C.R.T. terminal on which the type of fault occurred and valve involved are displayed.

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CHAPTER 1

INTRODUCTION

H.V.D.C. transmission is preferred to a.c. transmission for bulk power transfer and interconnections. While the earlier H.V.D.C. schemes used mercury arc rectifiers, the present installations use thyristor converters. The converters, in general, are prone to maloperations or faults due to internal problems or external causes. Since the converter operation dictates the performance of the d.c. link, it is necessary that the converter maloperations or faults be detected fast so as to initiate proper control action and to locate the fault quickly to minimize the repair time. This task can be accomplished through a properly designed and fast fault diagnostic system which can detect the nature of the converter maloperation. This information would also be extremely useful for the system operator.

1.1 CONVERTER FAULT DIAGNOSIS

The operation of converter valves follows a sequential and cyclic pattern within which, at all times, the conducting

state of each valve can be specified as ON or OFF. In the event of a converter fault, operation is either permitted to recover naturally or it is discontinued. In each case the normal logic pattern is disturbed and a subsequent unusual logic sequence develops. A normal logic sequence can be determined based on the ON/OFF state of the converter valves, firing pulse and a.c. voltage considerations. The sequential pattern of the valve conduction, as is known, can be related in time to the a.c. voltage waveforms and firing pulses.

A detailed analysis of the H.V.D.C. converter logic behaviour during normal and abnormal conditions has been reported in [1] which considers converter maloperations like arcbreak, arcthrough, quenching, misfire and commutation failure. The analysis illustrates each of these maloperations have a unique combination of the valve conduction pattern and governing time zones, which are bounded by the firing pulse regions and the voltage zero crossing of the a.c. supply. This forms a convenient basis for the fault detection. Based on this, the implementation of the fault detection scheme is reported in [2] using hardwired logic.

Although for control and protection the hardwired logic may have greater speed capability, the present trend is to

use microprocessors leading to reduced component count, better reliability and enhanced development flexibility. In this context microprocessor based fault diagnostic system is described in [3] for detection of certain faults primarily associated with the valve device. The detection of more frequently encountered faults in H.V.D.C. converters like commutation failure has not been attempted. The scheme uses ON/OFF detection based on valve currents. Dedicated hardware circuits have been used for the detection of the absence of a supply phase, short circuits across the thyristor as well as the d.c. terminals. A fast and reliable technique for the detection of the ON/OFF state of the valve is described in [4], based on the monitoring of gate to cathode voltage levels.

1.2 OBJECTIVE OF THE THESIS

The basic objective of the thesis is to develop a microprocessor based fault diagnostic system for H.V.D.C. converters. The detection procedure is based on the valve conduction status, firing pulse generated and a.c. voltage zero crossover instants [1]. Detection of the frequently encountered faults, viz., misfire and commutation failure has been implemented.

1.3 OUTLINE OF THE THESIS

The detailed description of various converter faults, viz., arcthrough, arcbback, misfire and commutation failure is given in Chapter 2. Also the basis for fault diagnosis has been established based on the valve conduction pattern, time zones governed by the pulse regions and the zero cross-over instants of the three phase supply.

The hardware realisation in order to derive the necessary information regarding the valve conduction status, presence of firing pulse produced by the converter control system, and the a.c. supply voltage regions has been discussed in Chapter 3 for the implementation of fault diagnostic scheme. The necessary interface of the detection circuits with the microprocessor workstation is also described in this chapter.

Chapter 4 discusses the software details for the implementation of microprocessor based fault diagnostic scheme. The detection of misfire and single commutation failure has been experimentally carried out using H.V.D.C. simulator to demonstrate the fault diagnostic system.

The conclusions and scope for further work are presented in Chapter 5.

CHAPTER 2

CONVERTER FAULTS AND DETECTION

Under normal operation the converter valves follow a sequential and cyclic pattern of conduction and cessation. Each valve conducts for a period of one third of the a.c. cycle and the overlap due to the converter transformer inductance. The duration of conduction and the pattern of conduction may, however, get disturbed during abnormal operation of converter. This abnormal operation of converter is often referred to as converter maloperation or fault, which may be due to internal problems of the converter or external causes arising in the d.c. link or the a.c. system connected to the converter. For effective design of converter control and protection strategies it is important to know the detailed behaviour of the converter during maloperation. In this chapter an attempt has been made in this direction to precisely detect the type of maloperation and the converter valve effected by it. The theoretical basis for the converter diagnostics is described.

2.1 NORMAL CONVERTER OPERATION

In H.V.D.C. transmission a.c. power is converted to d.c. through high power converters operating as rectifier and after transmission over the d.c. line, the d.c. power is converted back to a.c. through converters operating as inverter. Invariably d.c. transmission system has a bipolar configuration using 12-pulse converters at either ends. Each 12-pulse converter is made up of two 6-pulse bridge converters connected in series and fed with three phase a.c. supply 30° out of phase with each other, as shown in Fig. 2.1. The normal operation of 12-pulse converter depends on the normal operation of constituent 6-pulse converters.

Fig. 2.2 shows the 6-pulse bridge converter system. Under normal condition the valves are fired at regular intervals of 60° and the valve conduction pattern is 12, 123, 23, 234, 34, 345, 45, 456, 56, 561, 61, 612, 12. This indicates that the converter has an alternate two and three valve conduction. The duration of three valve conduction is known as overlap or commutation period, and arises as the current in the converter transformer winding cannot change instantaneously. Fig. 2.3 shows the voltage and current waveforms for 6-pulse bridge converter operating

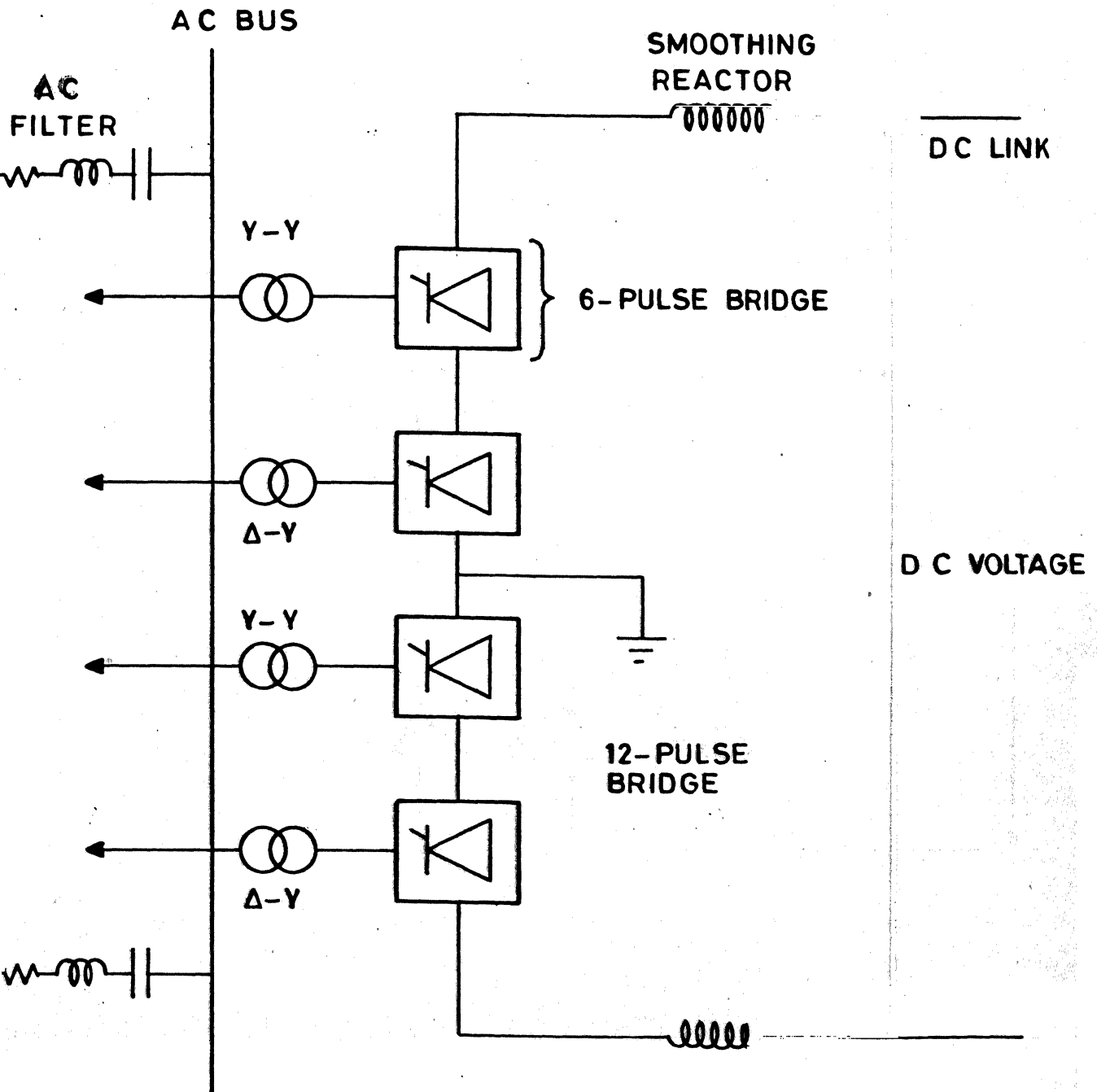


FIG. 2.1 INVERTER END OF H.V. D.C. LINK.

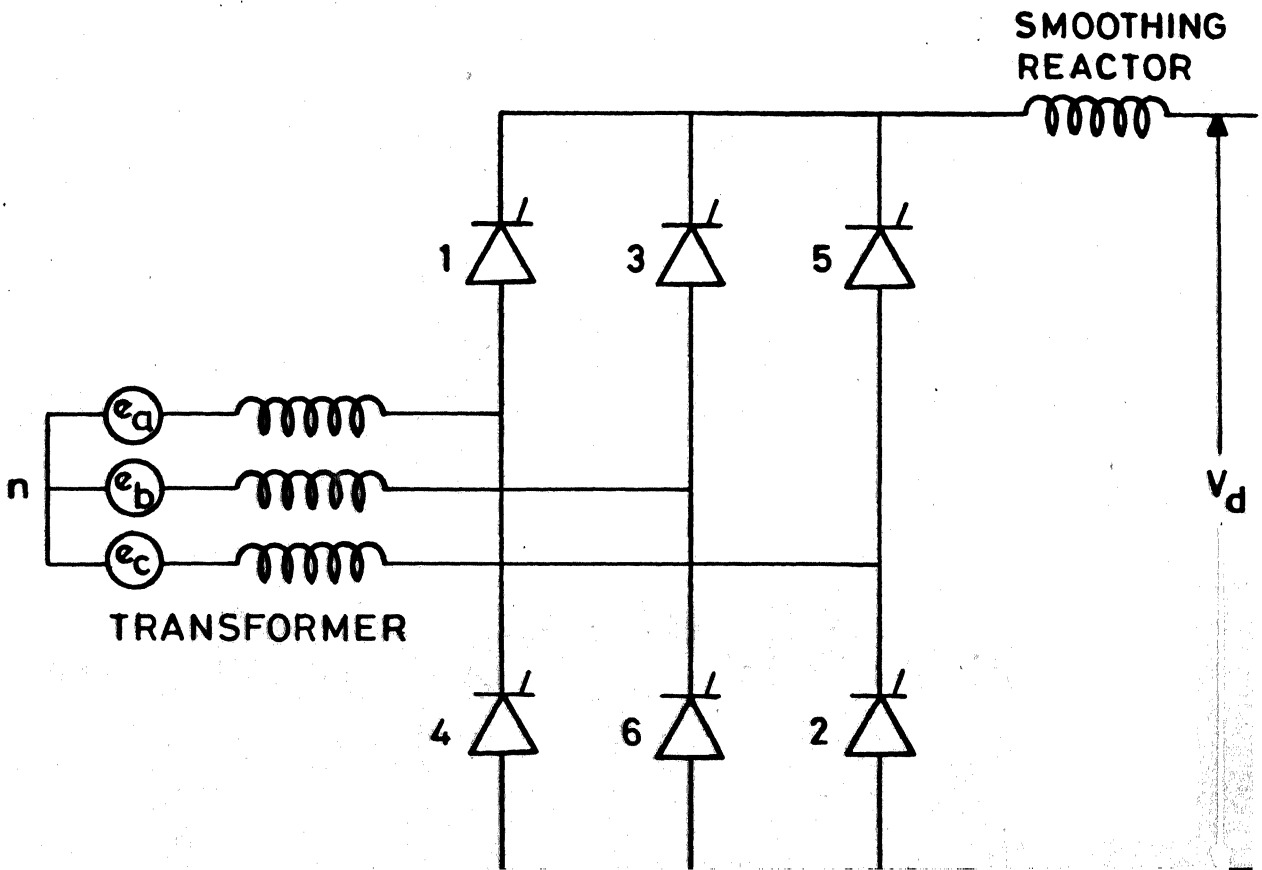


FIG. 2.2 SIX PULSE BRIDGE CIRCUIT

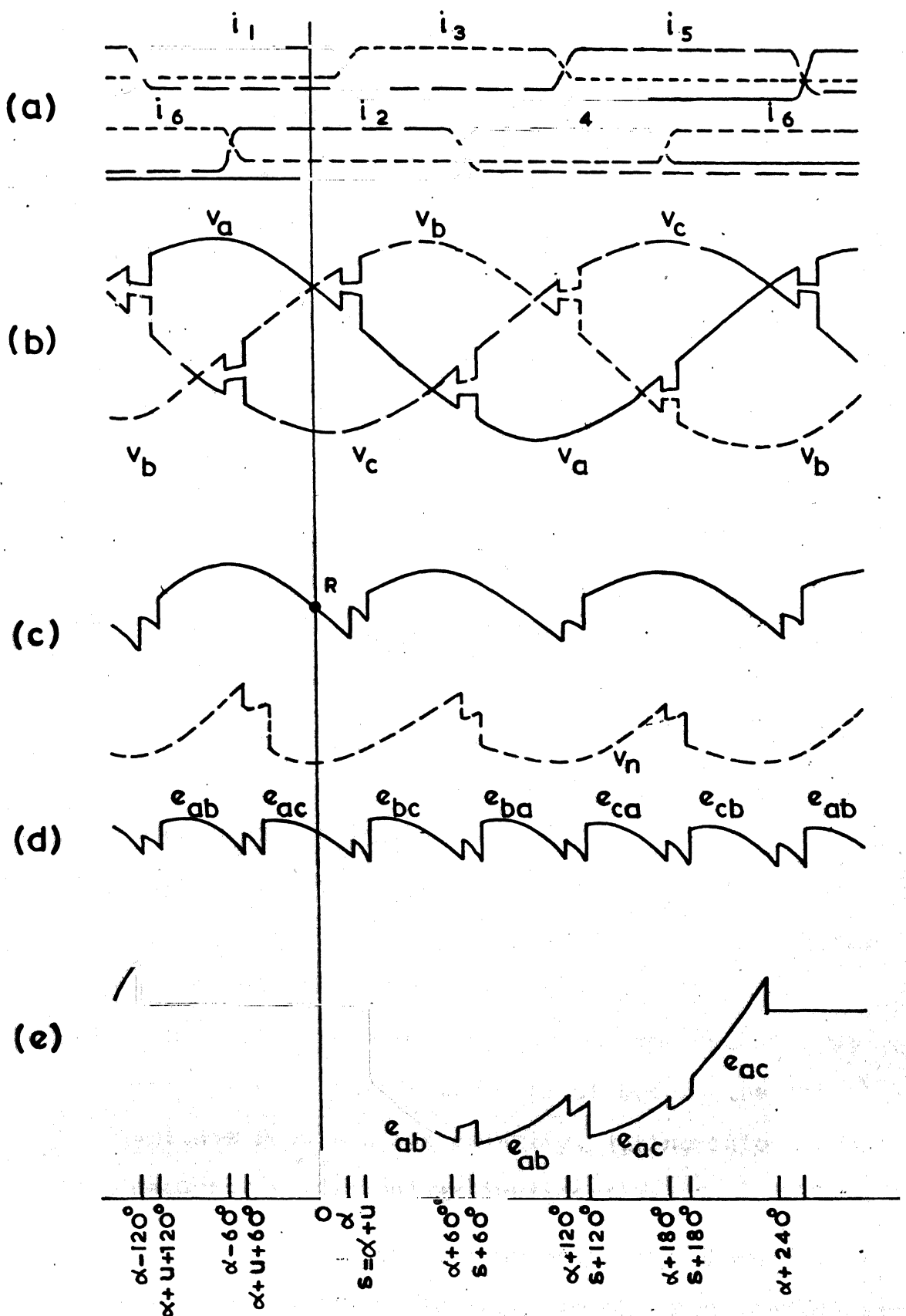


FIG.2.3 CURRENTS AND VOLTAGES OF 3 ϕ BRIDGE CONVERTER WITH $\alpha = 15^\circ$ AND $u = 15^\circ$ (a) VALVE CURRENTS (b) AC LINE TO NEUTRAL VOLTAGES (c) POLE VOLTAGES w.r.t. NEUTRAL (d) DIRECT VOLTAGE BETWEEN POLES

as rectifier with firing angle (α) equal to 15° and overlap angle (u) equal to 15° . As can be seen, the instant $\omega t = 0$ is defined at the crossing of the phase b and a voltages. Valve 3 triggers at the instant $\omega t = \alpha$. Fig. 2.4 shows voltage and current waveforms in case of inverter.

2.2 CONVERTER MALOPERATION

The various malfunctions or faults commonly encountered during converter operation are [5] :

- (a) arcbback - conduction in the reverse direction;
- (b) arcthrough - conduction during scheduled blocking period;
- (c) quenching - premature extinction of the conduction during the scheduled conduction period;
- (d) misfire - failure of the valve to fire during the scheduled conduction period; and,
- (e) commutation failure - failure of the incoming valve to take over the direct current before the commutating voltage reverses its polarity, taking into account need for sufficient extinction time.

The various periods during which the above faults occur are indicated in Fig. 2.5, which shows voltage across a valve during rectification and inversion. The cycle is divided into three periods, viz., inverse, blocking and

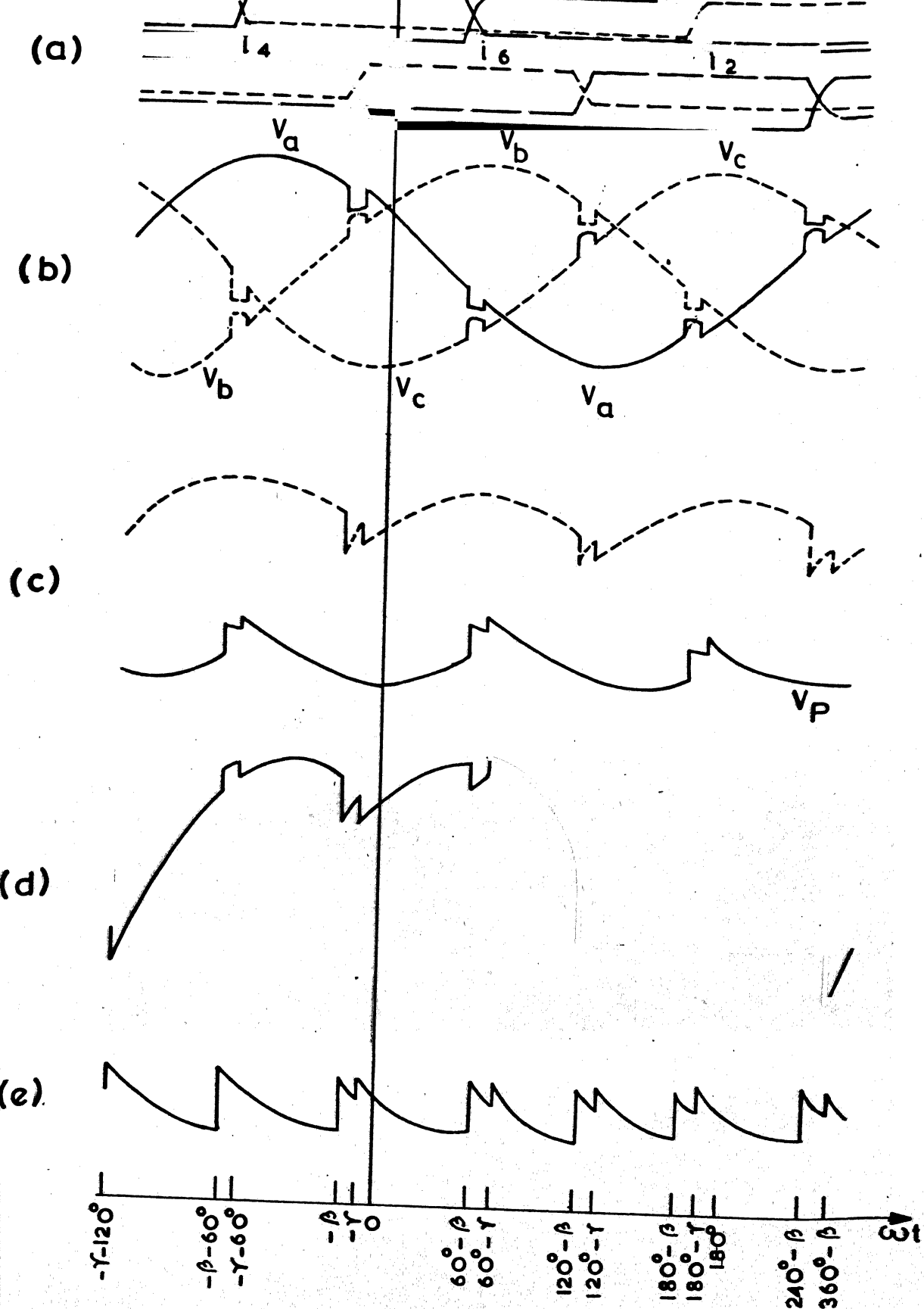


FIG. 2.4 CURRENTS AND VOLTAGES OF 3 ϕ BRIDGE INVERTER WITH $\alpha = 150^\circ$, $\beta = 30^\circ$, $u = 15^\circ$ AND $\gamma = 15^\circ$.
 (a) VALVE CURRENTS (b) LINE TO NEUTRAL AC VOLTAGES

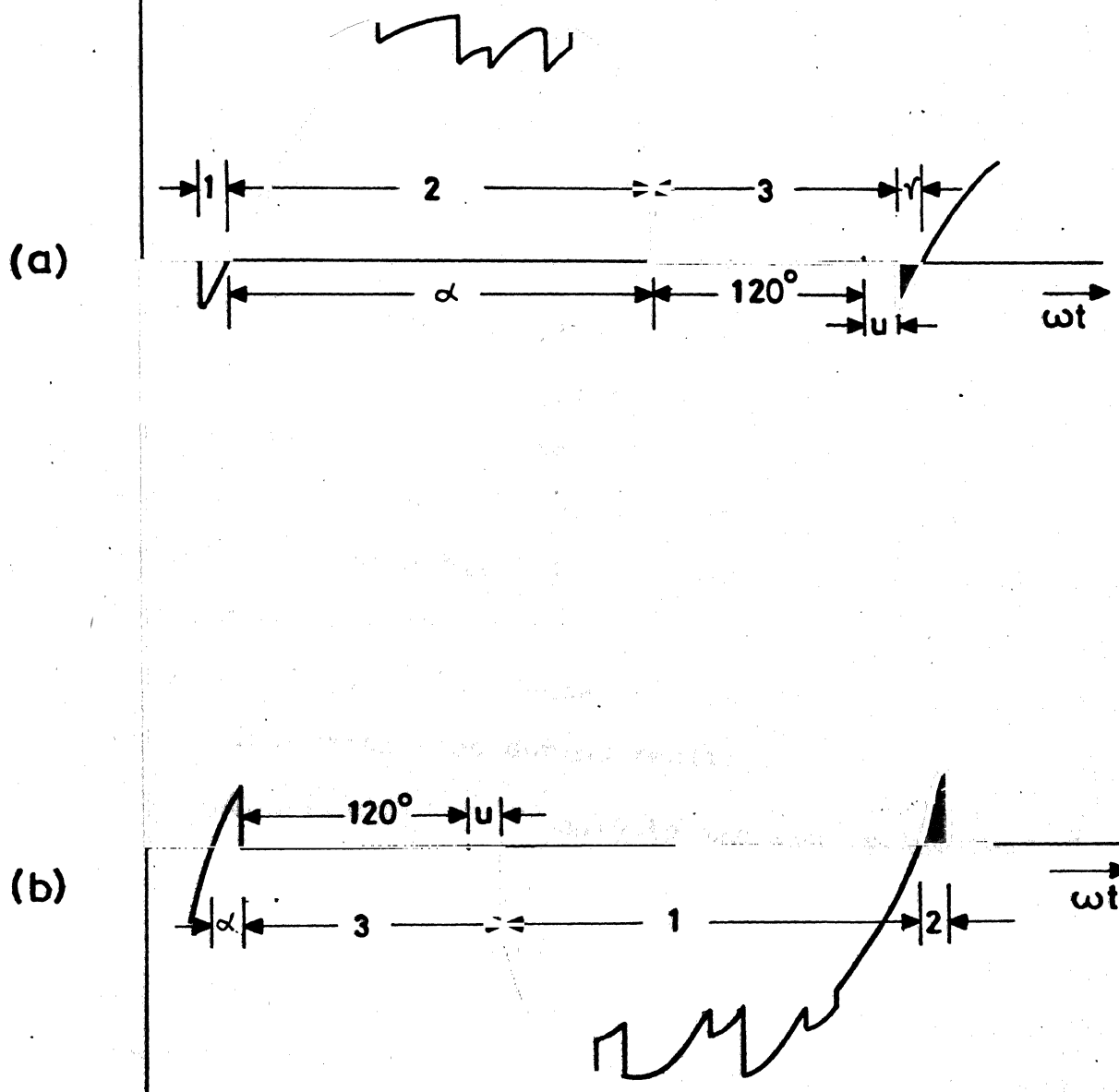


FIG.2.5 VOLTAGE ACROSS A VALVE IN.

(a) inverter and (b) rectifier.

1. inverse period 2. blocking period.

3. conducting period.

α . delay or firing angle.

γ . extinction angle.

conducting. The arcbreak of a valve can occur only in the inverse period. It is evident that rectifier valve has a longer inverse period and higher inverse voltage than that of the same valve during inversion. Hence arcbreaks are more frequent and more severe during rectification than during inversion, however, arcbreak is the possibility in case of mercury arc valves and not in case of thyristor valves. Arcthrough can occur only in the blocking period. An inverter valve has a longer blocking period and a higher forward voltage than that of the same valve during rectification (Fig. 2.5). Hence arcthroughs are more frequent during inversion than during rectification.

Quenching can occur only in the conducting period. Misfire can occur only at the beginning of scheduled conducting period. The commutation failure can occur during inversion, i.e., when firing angle is greater than 120° . The commutation failure is generally due to causes external to the converter viz., a low alternating voltage or high d.c. currents. Either of these conditions prevent completion of commutation process in sufficient time, as a result of which the direct current is shifted back from the incoming valve to the outgoing valve. The other converter maloperations are generally due to problems within the converter or

The behaviour of the converter during arcbreak, arc-through, commutation failure and misfire are shown in Figs. 2.6 to 2.10, primarily to illustrate the first occurrence of these faults and the valve conduction pattern subsequent to the fault. In these figures instants A, B, C, D, E and F denote the positive going zero crossings of the phase to phase supply voltages (commutating voltages) for valves 1 to 6 respectively. These correspond to the $\alpha = 0$ instants. P_1, P_2, \dots, P_6 denote the starting points of firing pulses for valves 1, 2, ..., 6 respectively, which are initiated by the control circuit. In each region formed by the voltage zeroes and starting of the firing pulses the conducting valves along with their conduction sequence are indicated, both under normal and fault conditions. For example, in Fig. 2.6 the conducting valves under normal operation in the region A- P_1 are 56. In the next region P_1 -B the conduction pattern under normal operation is shown as (5) 61. The valve number in the parenthesis indicates the valve which is going to cease conduction during this region.

Figs. 2.6 to 2.8 gives the valve conduction pattern after the first occurrence of arcbreak and arcbreak of valve 1, under different conditions of firing angle (α) and

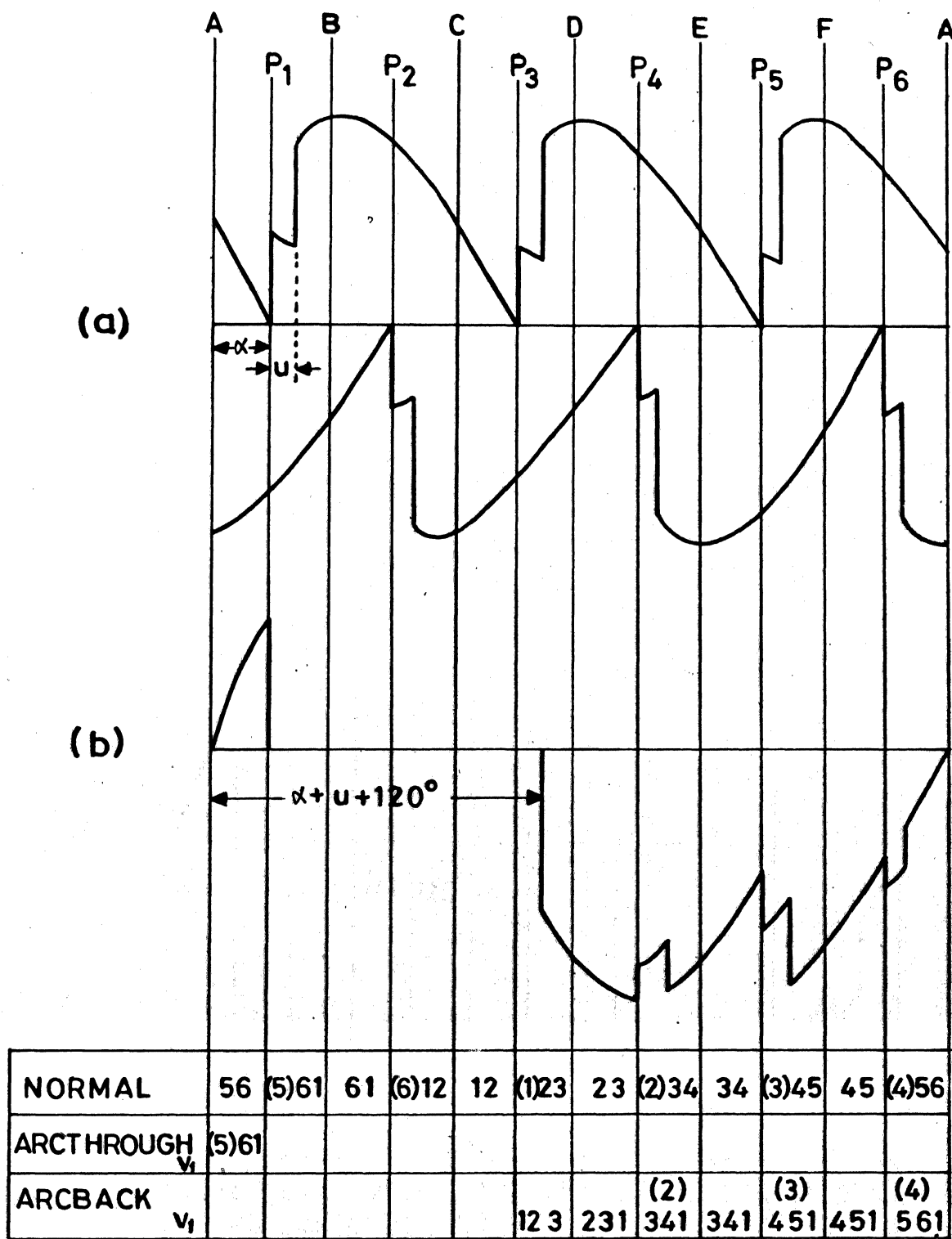


FIG. 2.6 ARCTHROUGH AND ARCBACK UNDER CONDITIONS $\alpha < 60^\circ$, $\alpha + u < 60^\circ$

(a) D.C. POLE VOLTAGES w.r.t. NEUTRAL OF a.c. VOLTAGE SOURCE.

(b) VOLTAGE ACROSS VALVE 1.

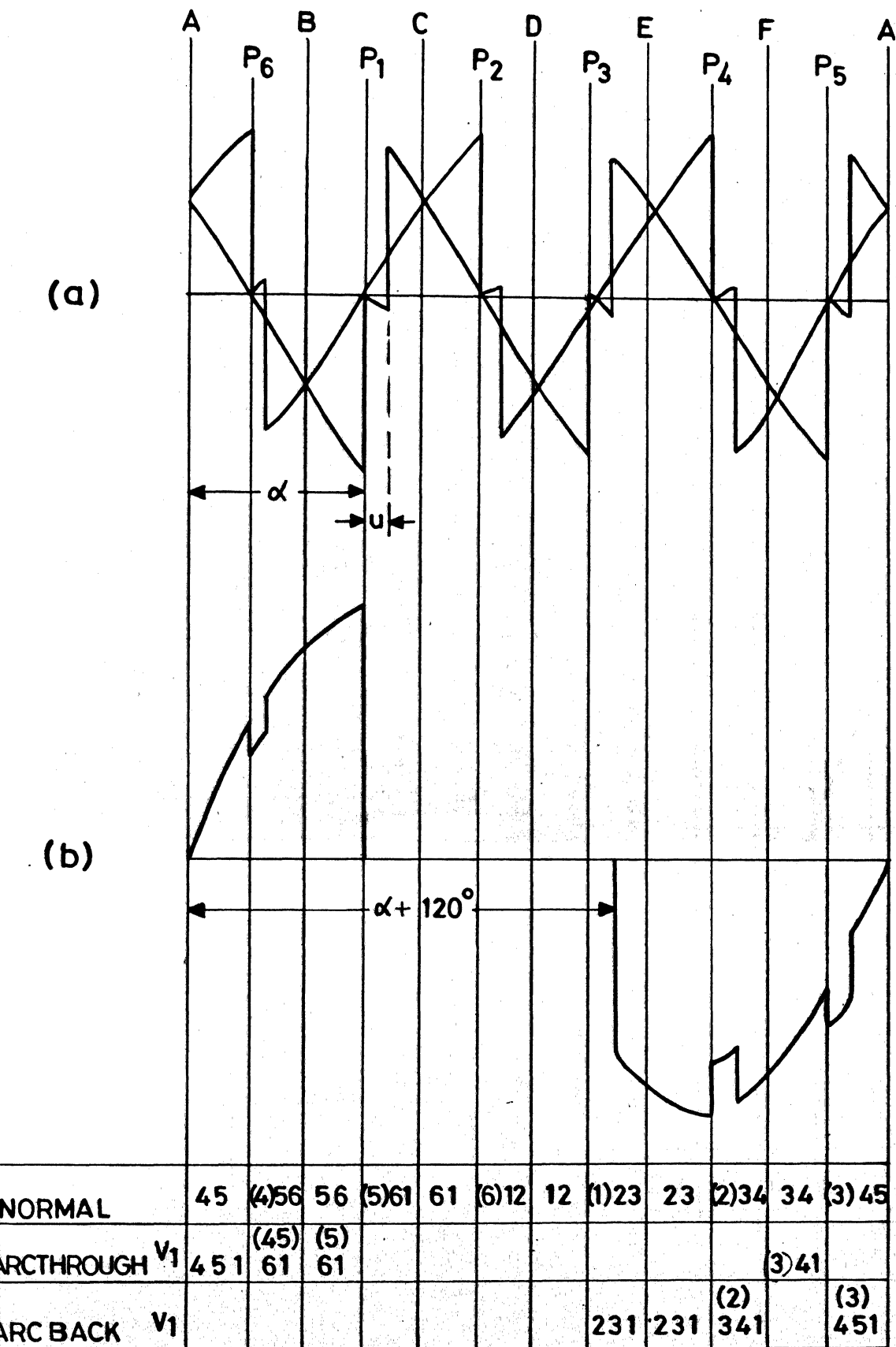


FIG. 2.7 ARCTHROUGH AND ARCBACK UNDER CONDITIONS $60^\circ < \alpha < 120^\circ, 60^\circ < \alpha + u < 120^\circ$

(a) D.C. pole voltages w.r.t neutral of a.c. source (b) voltage across valve

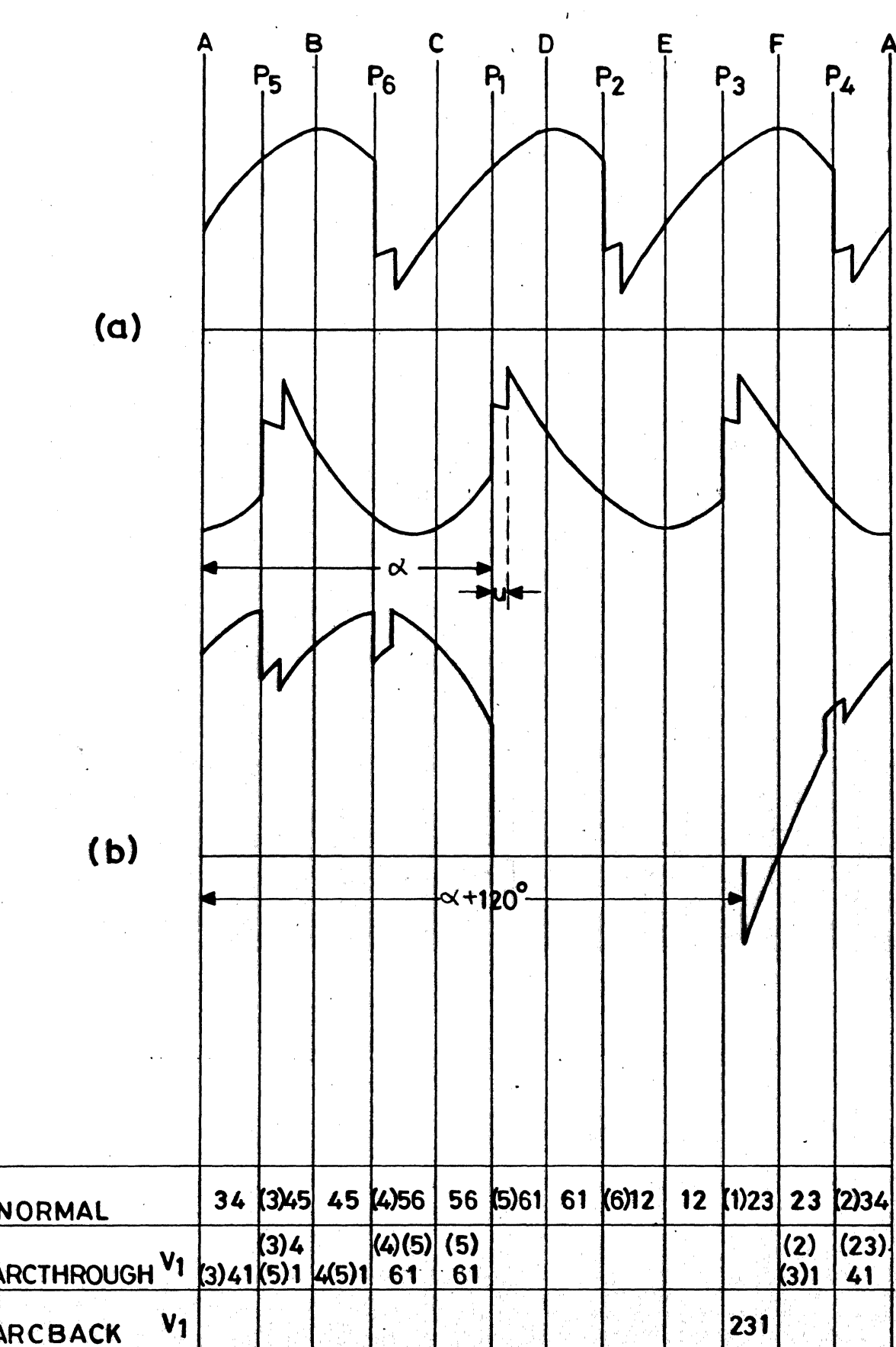


FIG. 2.8 ARCTHROUGH AND ARCBACK UNDER CONDITIONS $120^\circ < \alpha < 180^\circ, \alpha + u < 180^\circ$

(a) D.C. POLE VOLTAGES w.r.t. NEUTRAL OF A.C. SOURCE ,

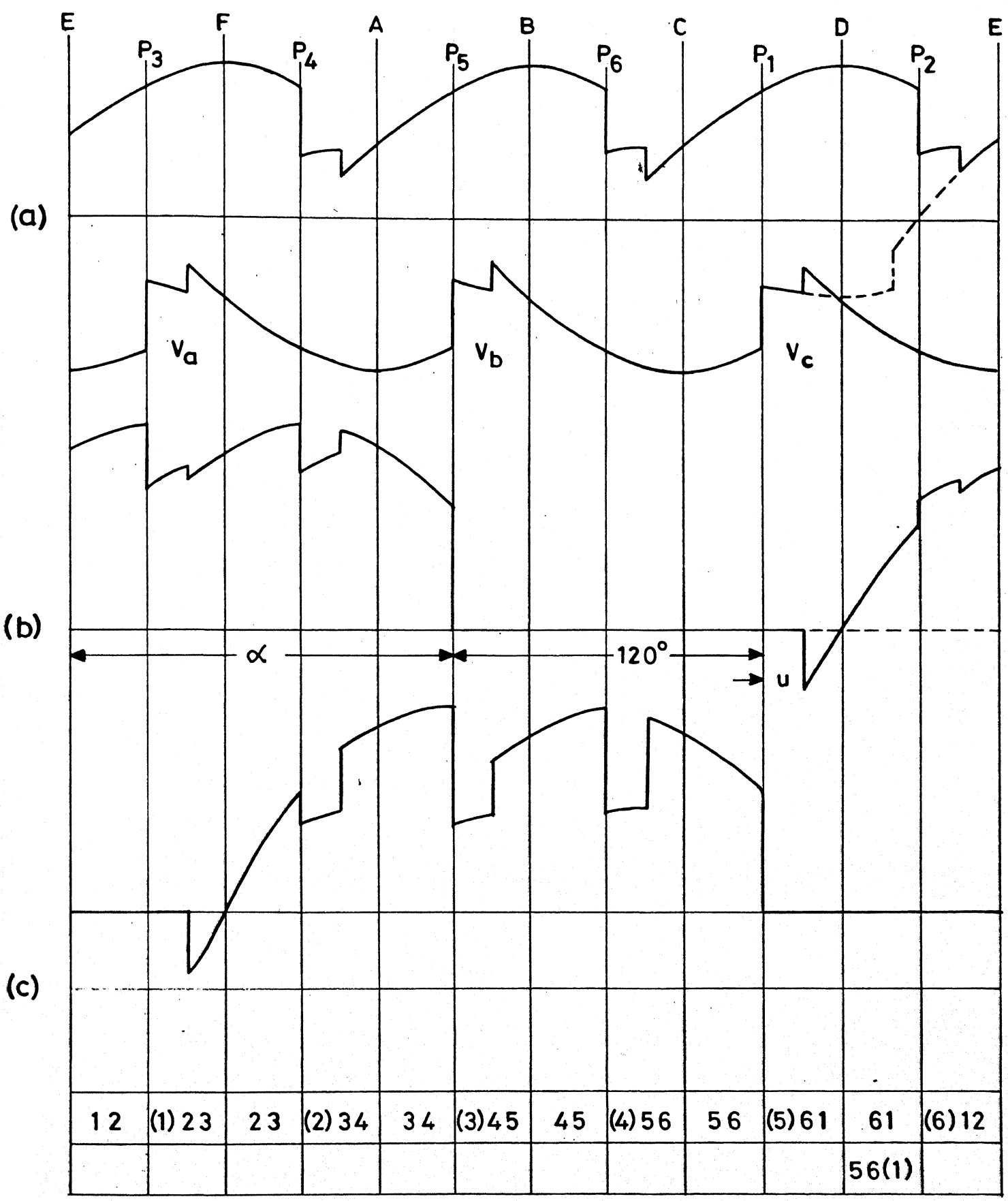


FIG.2.9 COMMUTATION FAILURE OF VALVE 5 TO 1

(a) POLE TO NEUTRAL VOLTAGES (b), (c) VOLTAGES ACROSS VALVE 5 AND 1.

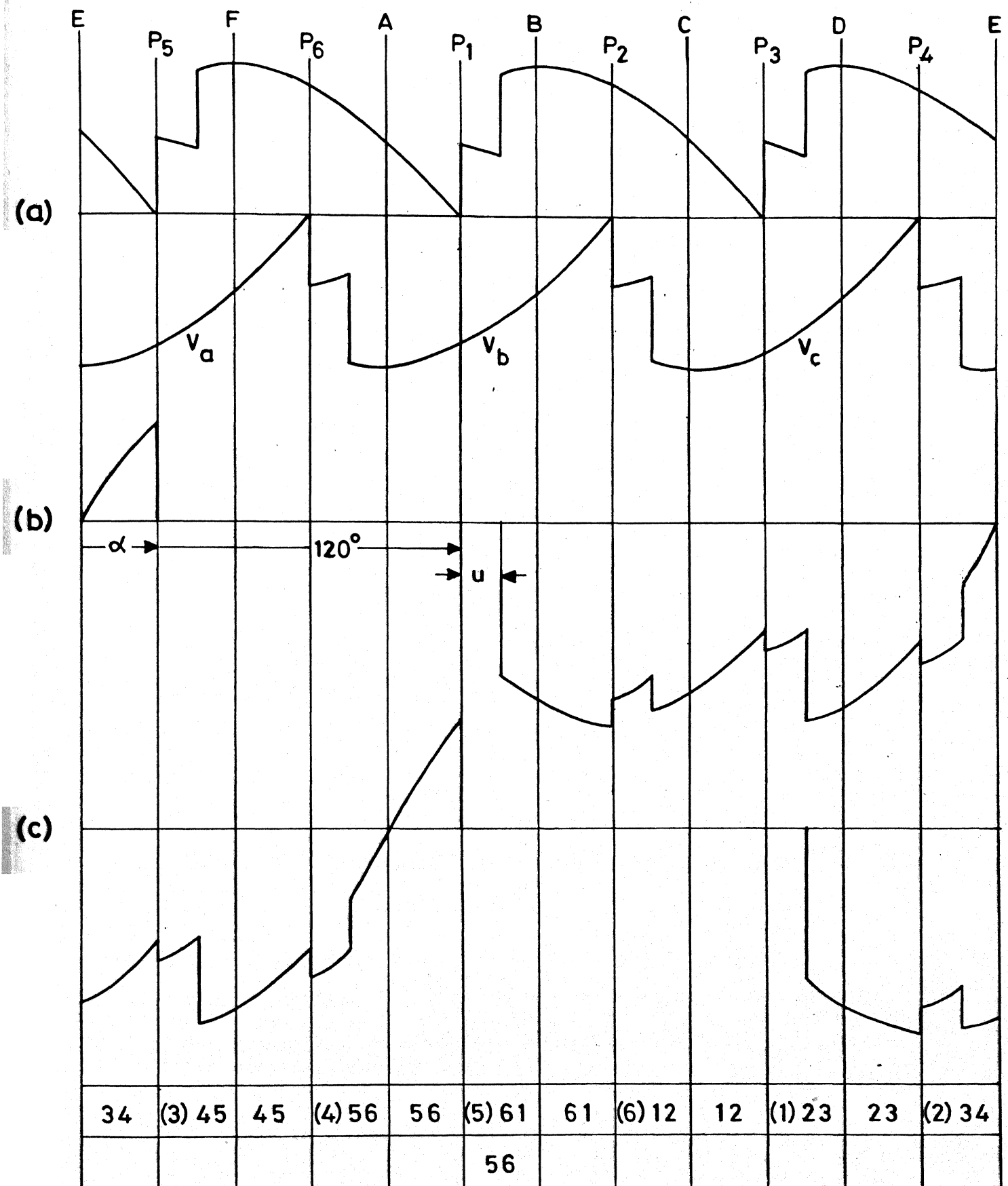


FIG. 2.10 MISFIRE OF VALVE 1.

(a) POLE TO NEUTRAL VOLTAGES (b), (c) VOLTAGES ACROSS VALVE 5 AND 1.

overlap angle (u). Waveforms (a) and (b) in these figures are respectively the d.c. pole voltages with respect to neutral of a.c. source and voltage across valve 1. Table (C) indicates the valve conduction pattern. It is evident, as described earlier, that arcbreak of a particular valve can occur during the time interval when the voltage across the valve is negative and arcbreak only when it is positive.

2.2.1 Arcbreak and Arcbreak

The voltage across valve 1 is positive during the voltage zones AB (Fig. 2.6(b)), AC, (Fig. 2.7(b)) and FA, AD (Fig. 2.8(b)). Hence it is evident that arcbreak of valve 1 can occur only in the region FD depending on the firing and overlap angles, which can vary over the range 0 to 180° . However, with the variation in the firing angle, the firing pulse initiation instants P_1 to P_6 would change positions relative to the voltage crossover instants A, B,... F. Thus for a particular value of firing angle, say $\alpha = 60^\circ$, the pulse region P_1P_2 would coincide with the voltage region BC. Likewise for $\alpha = 150^\circ$ the pulse region P_1P_2 would fall in voltage regions CD and DE. Hence, depending upon the firing angle a particular pulse region may fall in different voltage regions.

In Figs. 2.6 to 2.8 it can be observed that voltage across valve 1 is zero in the pulse region P_1P_3 . In the pulse region P_3P_4 the voltage across valve 1 can be either positive or negative depending on the value of α . It can be seen that the pulse region P_3P_4 will lie anywhere within the voltage region CA for α varying over the range 0 to 180° . As mentioned earlier, voltage across valve 1 will be positive in the voltage region FD. However, the pulse regions that fall within this voltage region may vary depending upon the firing angle. With reference to pulse region P_3P_4 , the arcthrough of valve 1 is possible only in the voltage region FA. Although in Fig. 2.8 it may appear that arcthrough of valve 1 is a possibility even in the region CD, it will be with reference to a different pulse region P_6P_1 and not with reference to P_3P_4 . Based on this it can, in general, be seen that corresponding to a particular pulse region there would only be a specific voltage region during which arcthrough of valve 1 is possible. Similarly, it can be seen that with reference to the pulse regions P_4P_5 , P_5P_6 , P_6P_1 the arcthrough of valve 1 is possible only in the voltage regions FB, FC and AD respectively.

Tables in the Figs. 2.6 to 2.8 show the valve conduction pattern under normal operation and after the first

occurrence of arcthrough of valve 1. Since in the pulse region P_3P_4 arcthrough of valve 1 can occur only in the voltage region FA, it can be seen in the table of Fig. 2.8 that the normal pattern in the region P_3P_4 , which is 23, changes to 2(3)1. In case of pulse region P_4P_5 , since arcthrough of valve 1 is possible in the region FB it can be observed from the table of Figs. 2.7 and 2.8 that normal conduction pattern 34 changes to (3)41 (Fig. 2.7) and normal pattern (2)34 or 34 changes to (23)41 or (3)41 respectively (Fig. 2.8). Similarly the changes in the valve conduction pattern, following the arcthrough of any valve can be derived based on the knowledge of the pulse region and the corresponding voltage regions [1].

The arcbback of a valve can occur only when there is a reverse voltage across it. In Figs. 2.6 to 2.8 it can be noticed that for a variation of α from 0 to 180° the duration of reverse voltage across valve 1 lies in the voltage region CA. Once again, as in the case of arcthrough, the voltage across valve 1 is zero in the pulse region P_1P_3 . The pulse region P_3P_4 , although can fall in the voltage region CA, the arcbback of valve 1 will occur only in the voltage regions CE (Fig. 2.6(b)) or DF (Fig. 2.7(b)) or EF (Fig. 2.8(b)) depending upon the value of α .

This indicates that with reference to pulse region P_3P_4 the arcbback of valve 1 can occur only in the voltage region CF. With reference to pulse region P_3P_4 , this establishes the uniqueness in the occurrence of arcbthrough and arcbback of valve 1. While the former occurs in the voltage region FA the latter occurs in the voltage region CF. Similarly, for the arcbback of other valves the corresponding pulse and voltage regions can be determined. As in the case of arc-through, the different valve conduction patterns following arcbback of any valve can be derived as shown in the Tables of Figs. 2.6 to 2.8.

2.2.2 Commutation Failure and Misfire

Fig. 2.9 shows the voltage waveforms to explain the process of commutation. For valve 5 the $\alpha = 0$ instant coincides with point E, the positive going zero crossing of valve 5 commutation voltage V_{cb} . As is evident valve 5 can start conduction anywhere in the region EB. After the beginning of conduction valve 5 continues to conduct for a period of $(120 + u)$ degrees (Fig. 2.9(b)). During this period valve 1 starts conducting at the instant $(\alpha + 120)$ degrees, i.e., at the instant P_1 . For successful commutation valve 5 should cease conduction at the instant $(\alpha + 120 + u)$ degrees, which is less than 300° (instant D), as voltage

across valve 5 becomes positive beyond this instant. If this does not happen valve 5 continues to conduct and valve 1 would cease conduction, thus resulting in commutation failure of valve 1. It can be observed that commutation failure of valve 1 will take place in the pulse region P_1P_2 only when the corresponding voltage region is DE. As shown in the table of Fig. 2.9 the conduction pattern in the region DP_2 changes to 56(1) from normal pattern 61. Similarly, the commutation failure of the valves 2,3,4,5 and 6 can be determined with respect to pulse regions P_2P_3 , P_3P_4 , P_4P_5 , P_5P_6 and P_6P_1 respectively.

Fig. 2.10 gives the voltage waveforms to describe the occurrence of misfire of a valve. Valve 5 starts conduction at instant P_5 and continues to conduct for a period of $(120 + u)$ degrees (Fig. 2.10(b)). Valve 1 can start conduction anywhere between its positive going zero crossing instant and an instant 180° later (instant D), i.e., valve 1 can conduct anywhere in the region AD. From Fig. 2.10(c) valve 1 starts conduction at instant P_1 when voltage across it is positive. In case of misfire, valve 1 does not start conduction at all. As a result, in the pulse region P_1P_2 the conduction pattern becomes 56 instead of the normal pattern (5)61 (refer to table of Fig. 2.10). The voltage

region in which misfire of valve 1 can occur is the whole region AD. Similarly, it can be derived that the misfire of valves 2,3,4,5 and 6 can occur in the pulse regions P_2P_3 , P_3P_4 , P_4P_5 , P_5P_6 and P_6P_1 respectively with the corresponding voltage regions as BE, CF, DA, EB and FC.

2.3 BASIS OF CONVERTER FAULT DETECTION

In the preceding sections the first occurrence of various converter faults has been described in detail for valve 1 with reference to the pulse regions, corresponding voltage regions and valve conduction patterns. Similarly, detailed investigations can be carried out for different converter faults involving other valves. These results can be combined together in the form of generalised fault table [1] shown in Table 2.1. This table, at the outset, shows the normal conduction pattern and the corresponding effective voltage regions in the various pulse regions. As mentioned earlier, the arctrough of valve 1 can occur only in a specific subregion of the voltage region FD, provided that there is a specific valve conduction pattern during this subregion. For example, if the pulse region under consideration is P_4P_5 and the voltage subregion FB, then conduction pattern of (2341 indicates arctrough of valve 1.

Table 2.1 Generalised fault table

	P ₁ -P ₂	P ₂ -P ₃	P ₃ -P ₄	P ₄ -P ₅	P ₅ -P ₆	P ₆ -P ₁
normal	(5)61 AE	(6)12 BF	(1)23 CA	(2) 34 DB	(3) 45 EC	(4)56 FD
V ₁			2(3)1 FA	(23)41 FB	(3)4(5)1 FC	(45)61 AD
V ₂	(56)12 BE			3(4)2 AB	(34)52 AC	(4)5(6)2 AD
Arc- through	(5)6(1)3 BE	(61)23 CF			4(5)3 BC	(45)63 BD
V ₃	(56)14 CE	(6)1(2)4 CF	(12)34 DA			5(6)4 CD
V ₄	6(1)5 BDE	(61)25 DF	(1)2(3)4 DA	(23)45 EB		
V ₅		1(2)6 EF	(12)36 EA	(2)3(4)6 EB	(34)56 FC	
V ₆						
V ₁			231 CF	(2)3 41 DF	(3)4 51 EA	(4)561 FA
V ₂	(5)612 AB			342 DA	(3)452 EFA	(4)562 FB
Arc- back	(5)613 AC	(6)123 BC			453 EB	(4)563 FB
V ₃	(5)614 AC	(6)124 BD	(1)234 CD			564 FC
V ₄	615 AD	(6)125 BD	(1)235 CE	(2)345 DE		
V ₅		126 BE	(1)236 CE	(2)346 DF	(3)456 EF	
V ₆						

Table 2.1 (contd. . .)

Misfire of V ₁ -V ₆	56 AD	61 BE	12 CF	23 DA	34 EB	45 FC
s.c.f. of V ₁ -V ₆	56(1) CE	61(2) DF	12(3) FA	23(4) FB	34(5) AC	45(6) BD
Arcquenching	(5)(6)(1) AE	(6)(1)(2) BF	(1)(2)(3) CA	(2)(3)(4) DB	(3)(4)(5) EC	(4)(5)(6) FD
	(5)(1)(6)	(6)(2)(1)	(1)(3)(2)	(2)(4)(3)	(3)(5)(4)	(4)(6)(5)

Likewise, it can be observed that for an arcthrough of any valve there is a complete uniqueness as far as the pulse region, voltage region and conduction pattern are concerned. Similar observations can be made for other kinds of faults. This feature of uniqueness forms the basis for the detection of converter fault. Moreover, it can be observed that within a particular pulse region, even though the conducting valves may be the same, the fact that the corresponding effective voltage regions are different is indicative of different nature of faults.

From the generalised fault table it is evident that in order to detect any converter fault and the valve involved therein it is important to have knowledge regarding conducting valves, pulse regions and the voltage regions. A unique combination of these as shown in the table will indicate a particular fault and the valve concerned.

2.4 CONCLUSIONS

In this chapter a detailed investigation into various converter faults has been carried out. A particular fault of a valve can occur in a particular pulse region, provided in the corresponding voltage region there is a specified valve conduction pattern. This unique feature of converter

faults forms the basis for fault detection. Detection of any fault, therefore, requires information regarding various pulse regions, voltage regions and the ON/OFF states of valves. The next chapter describes the hardware details for obtaining these information.

CHAPTER 3

HARDWARE REALISATION OF FAULT DETECTION SCHEME

The block diagram of the fault diagnostic system is shown in Fig. 3.1. As discussed in the previous chapter three types of signals are needed to implement the detection scheme, viz., firing pulse signals, voltage region signals and ON/OFF states of the valves. The six firing pulse signals from the control circuit are accessed by the gate pulse detector which outputs the firing pulse signals at appropriate digital levels and with proper isolation from the control circuit. The voltage region signals are obtained by voltage region detector, which taps the three stepped down and isolated line voltages (commutation voltages of valves) from the converter. It digitises them to the appropriate logic levels. The ON/OFF signals of valves are obtained from ON/OFF detection circuit which taps the six valve currents in the converter bridge using current sensing transducers, digitising to the appropriate logic level and isolated using opto-

isolators. These three types of signals are fed to the I/O interface consisting ports and interrupt generator. The I/O interface gives an interrupt at the start of every firing pulse to the microprocessor workstation, which is built around microprocessor 8085. The processor in the workstation gets interrupted at each occurrence of interrupt signal and accesses the voltage and ON/OFF information from I/O interface. This information is passed as input data to the resident fault detection software. The software checks for the occurrence of faults, if any, and displays the type of fault and valve involved on the workstation monitor. In case, no occurrence of fault is detected a message is flashed on the monitor screen stating that the converter is under normal operation. This type of monitoring scheme is extremely useful for the operator at the terminal station.

The details and the working of various blocks in Fig. 3.1, viz., firing pulse detector, voltage region detector, ON/OFF detection circuit and I/O interface are described in the following sections.

3.1 FIRING PULSE DETECTOR

The circuit diagram of the scheme for pulse detection is given in Fig. 3.2 and the corresponding waveforms in

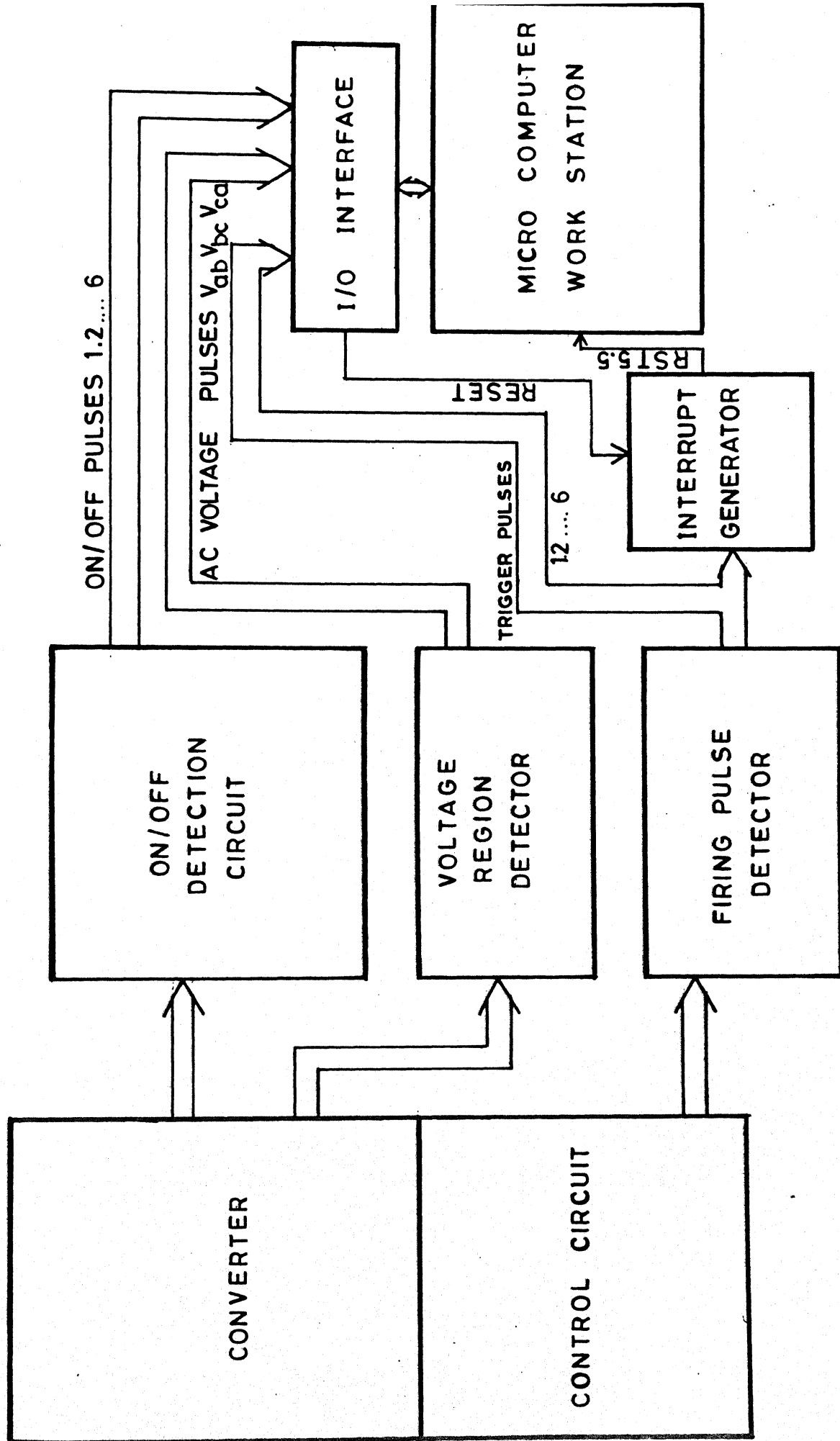


FIG.3.1 BLOCK DIAGRAM OF μP BASED FAULT DIAGNOSTIC SYSTEM.

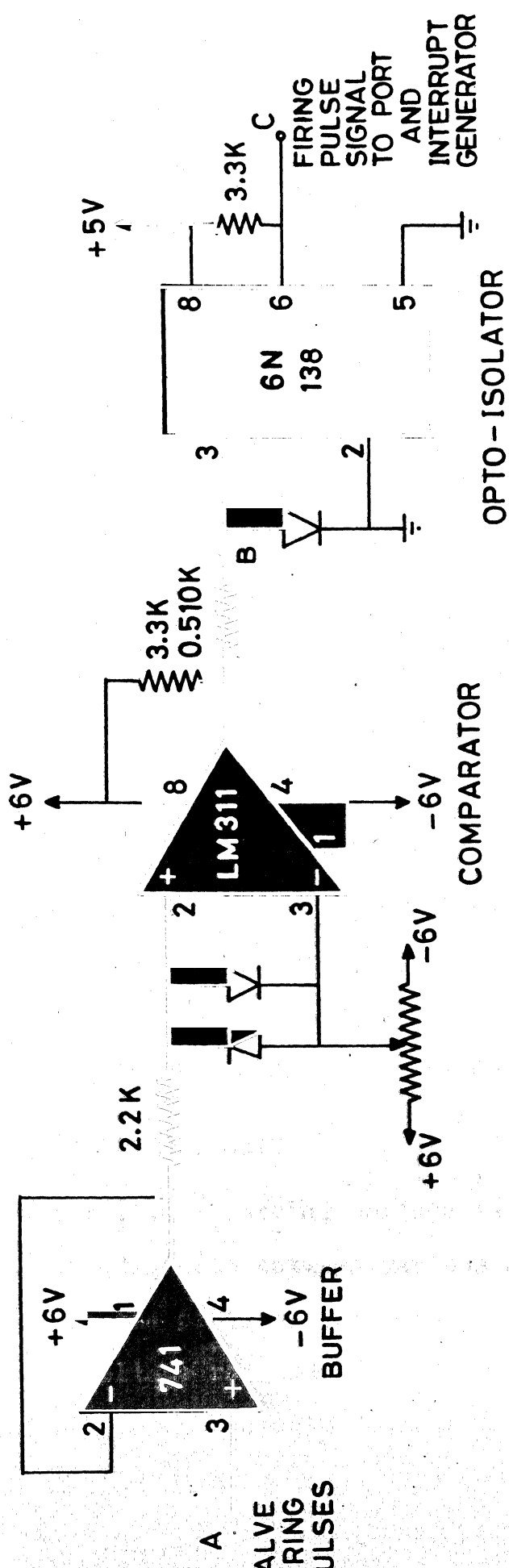


FIG. 3.2 THE PULSE DETECTOR

Fig. 3.3. The firing pulse from the firing generator of the converter is given as the input to the buffer (point A). The firing pulse waveform is shown in Fig. 3.3a. The output of buffer is fed to a comparator which gives a low output (point B) when input is between zero to $-3V$. This signal level at the input of comparator can be adjusted using the potentiometer depending upon the level of the firing pulse obtained from the converter control circuit. The comparator output is isolated and inverted by opto-isolator to give a high output (point C) indicating the presence of the pulse. The outputs at points B and C are shown in Fig. 3.3b and c respectively. If the input to the comparator is more negative than $-3V$ the output of comparator is high and the output of opto-isolator becomes low indicating absence of firing pulse. Six such circuits are used to detect all six firing pulse signals.

3.2 VOLTAGE REGION DETECTOR

The information regarding voltage region is essential in order to discriminate between various converter faults as described in the previous chapter. In each a.c. cycle there are six voltage regions of interest each having a duration of 60° under balanced conditions. These six

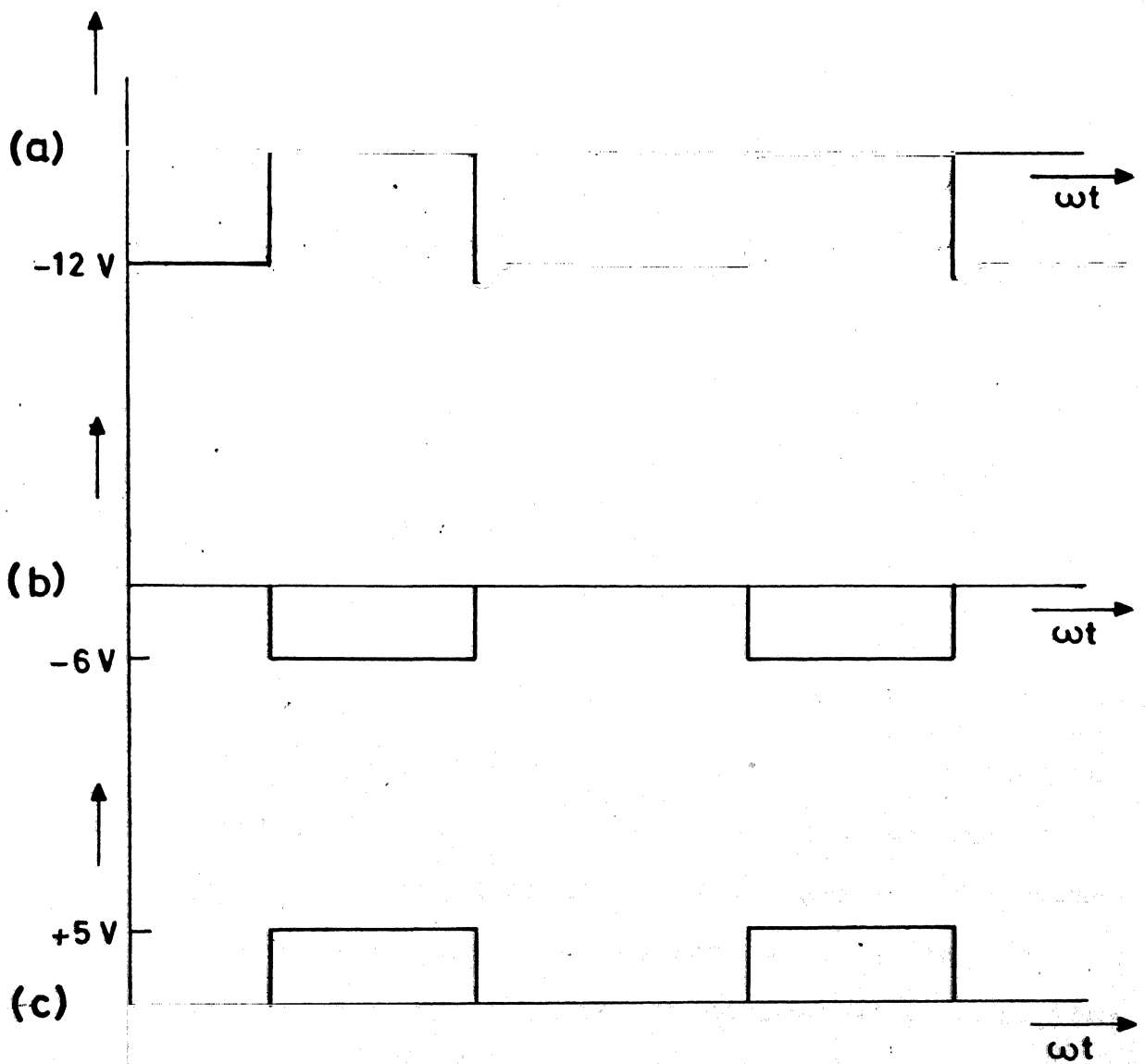


FIG.3.3 WAVE FORMS OF PULSE DETECTOR.

(a) firing pulse (input)

(b) output of comparator

(c) output of optoisolator

voltage regions in fact correspond to the regions between successive zero crossing of the valve commutation voltages (refer to Chapter 2). The valve commutation voltages are derived from the three line to line voltages of the supply system connected to the converter. The detection of the voltage region is based on the digitised version of stepped down line to line three phase a.c. voltages. The detection circuit is shown in Fig. 3.4 and the corresponding output signals in Fig. 3.5. Each of the three line to line voltages is fed to a comparater which gives an output low when line voltage is positive. This in turn makes the output of opto-isolator high, indicating the positive nature of the line voltage (ref. Fig. 3.5(b)). The digitised versions of the three line to line voltages are then combined at the input ports (in the form as shown in the table of Fig. 3.5 to result in six desired voltage regions AB, BC, ..., FA. In the region AB, the pattern 100, which is obtained as a combination of the digitised line to line voltages, indicates that the line to line voltage v_{ab} is high and the other line to line voltages are low. The present scheme enables to derive the voltage region information precisely even if the supply voltages are unbalanced.

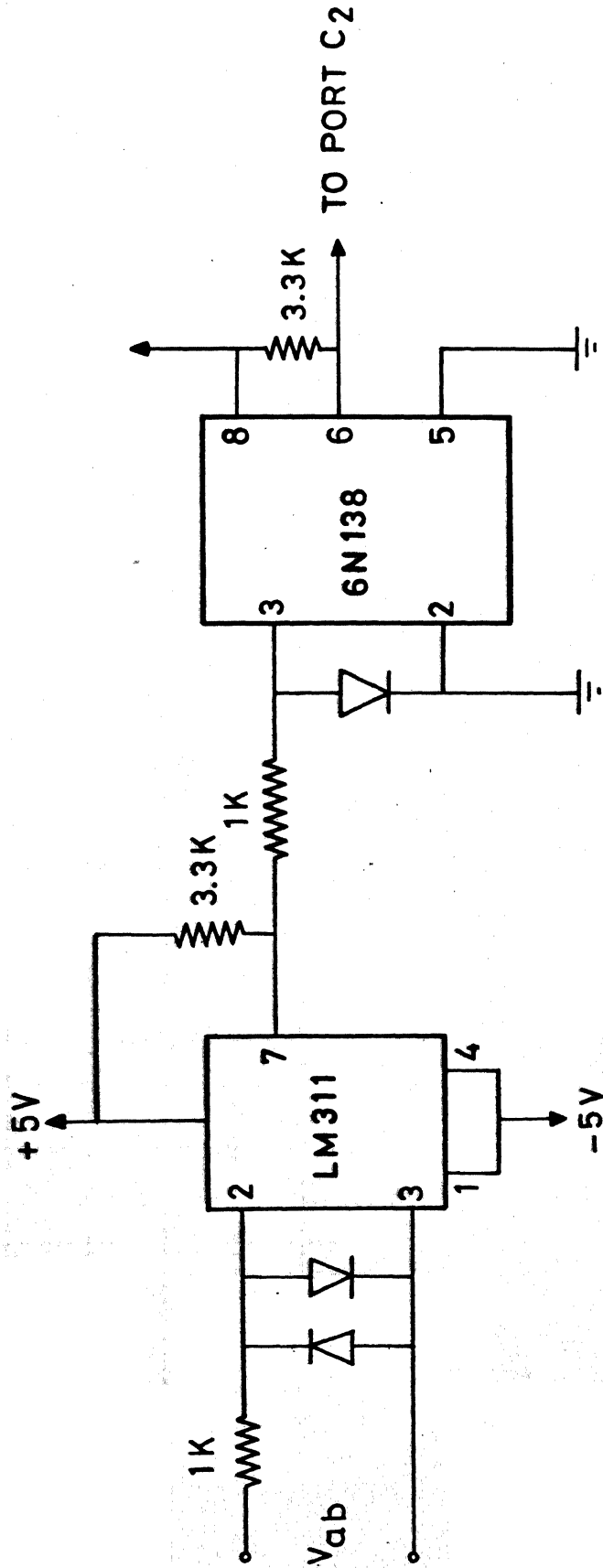


FIG. 3.4 VOLTAGE REGION DETECTOR

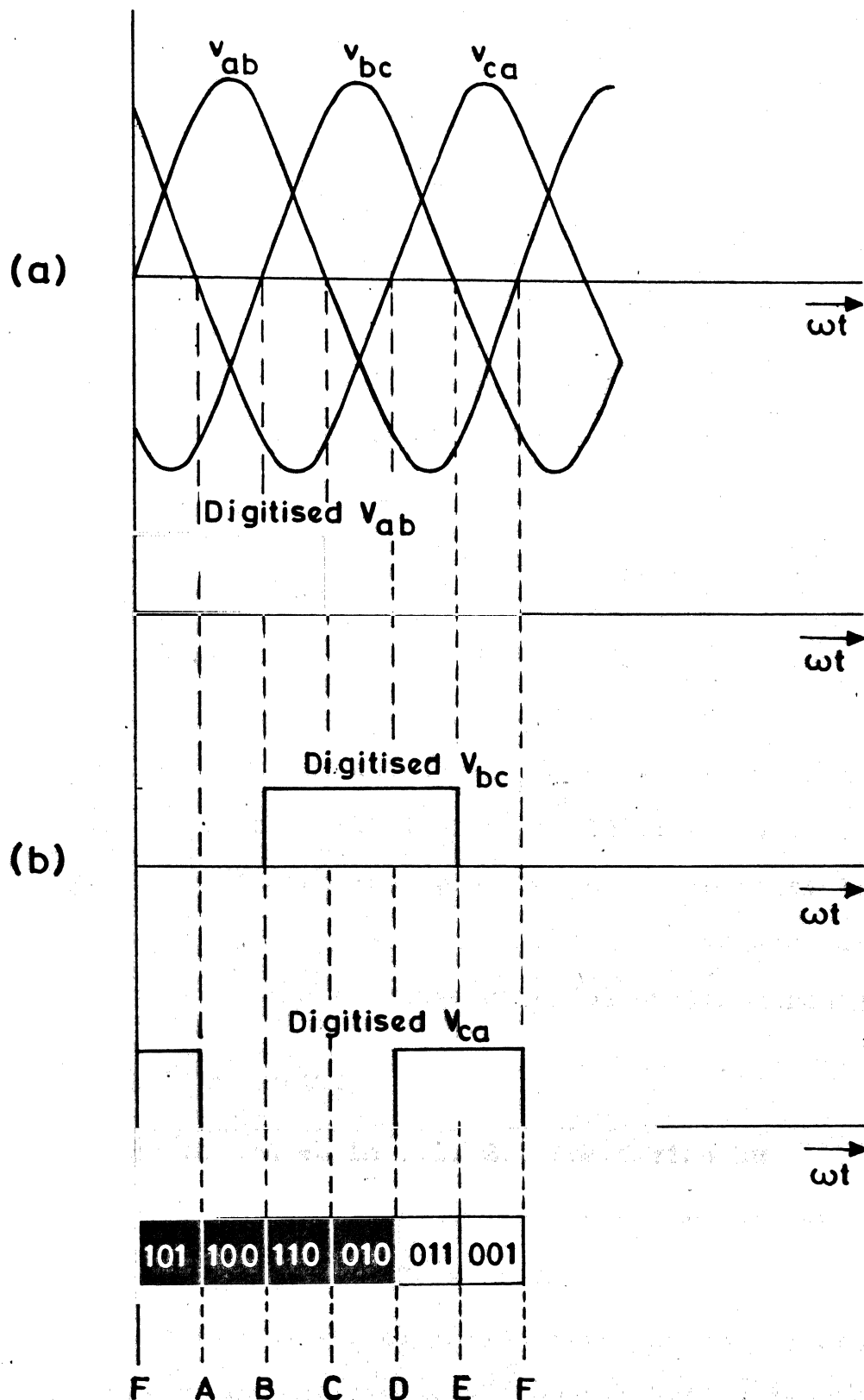


FIG.3.5 OUTPUT OF VOLTAGE REGION DETECTOR.

(a) line to line commutation voltages.

(b) digitised commutation voltages.

3.3 ON/OFF STATUS DETECTOR

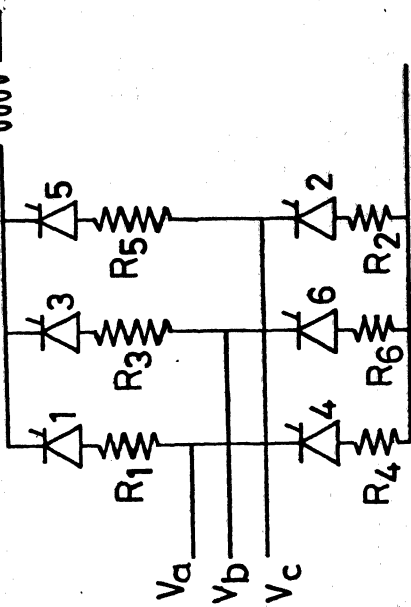
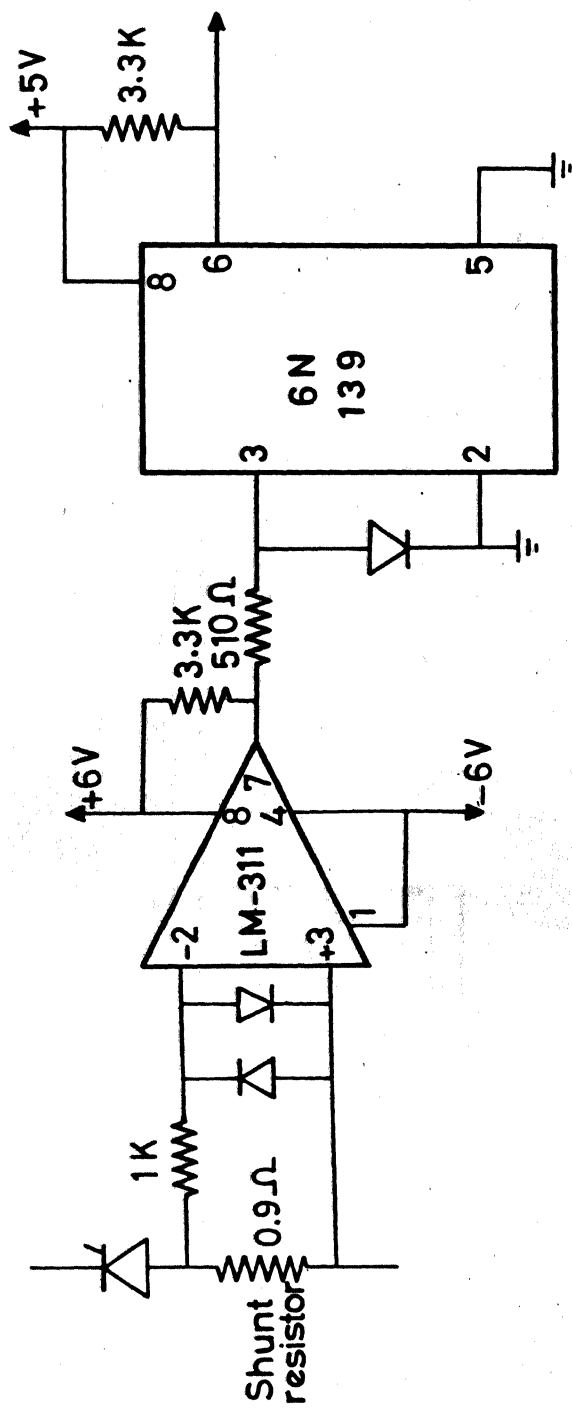
Information regarding the ON/OFF status of the valve is essential to establish the type of fault in a converter.

The circuit diagram to accomplish this is given in Fig. 3.6. A low value shunt is connected in series with each valve. The voltage across this shunt is given as input to the comparator adjusted to be in negative saturation. This gives a low state at the output of opto-isolator indicating valve OFF state. Similarly a current through the shunt as low as one percent of rated current gives a high state at the output of opto-isolator indicating the ON state of the valve. Opto-isolators provide complete isolation between the power and detection circuits. To achieve further isolation floating power supplies are used for positive and negative group detection circuits.

3.4 I/O INTERFACE

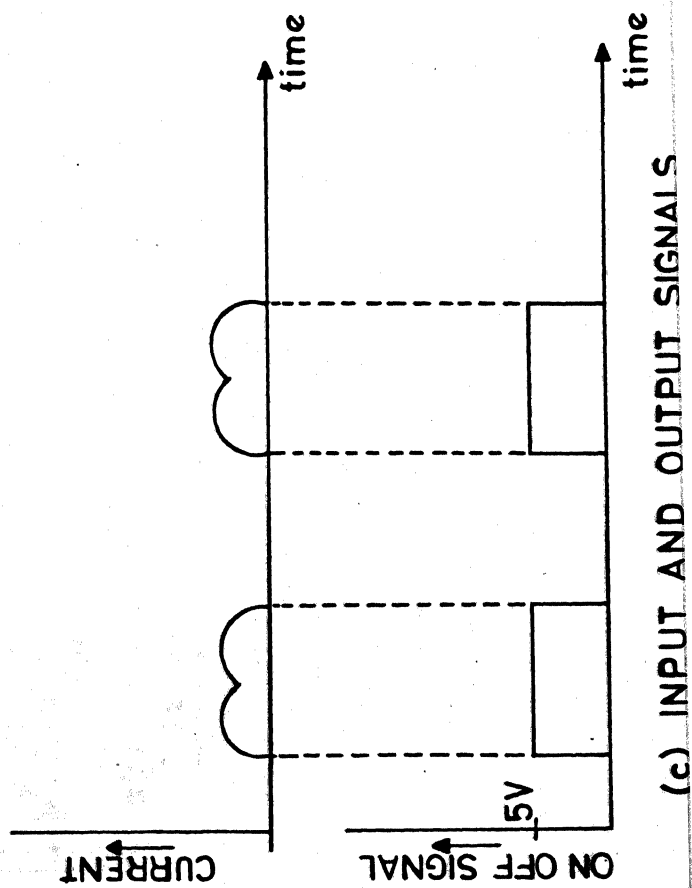
As indicated in Fig. 3.1 the firing pulse signals, voltage region signals and ON/OFF status are fed to the I/O interface of the workstation.

The I/O interface realisation and the various subsystems of workstation are shown in Fig. 3.7. The six firing pulse signals from the pulse detector are fed to the



(a) CONVERTER

(b) ON-OFF DETECTOR CIRCUIT



(c) INPUT AND OUTPUT SIGNALS

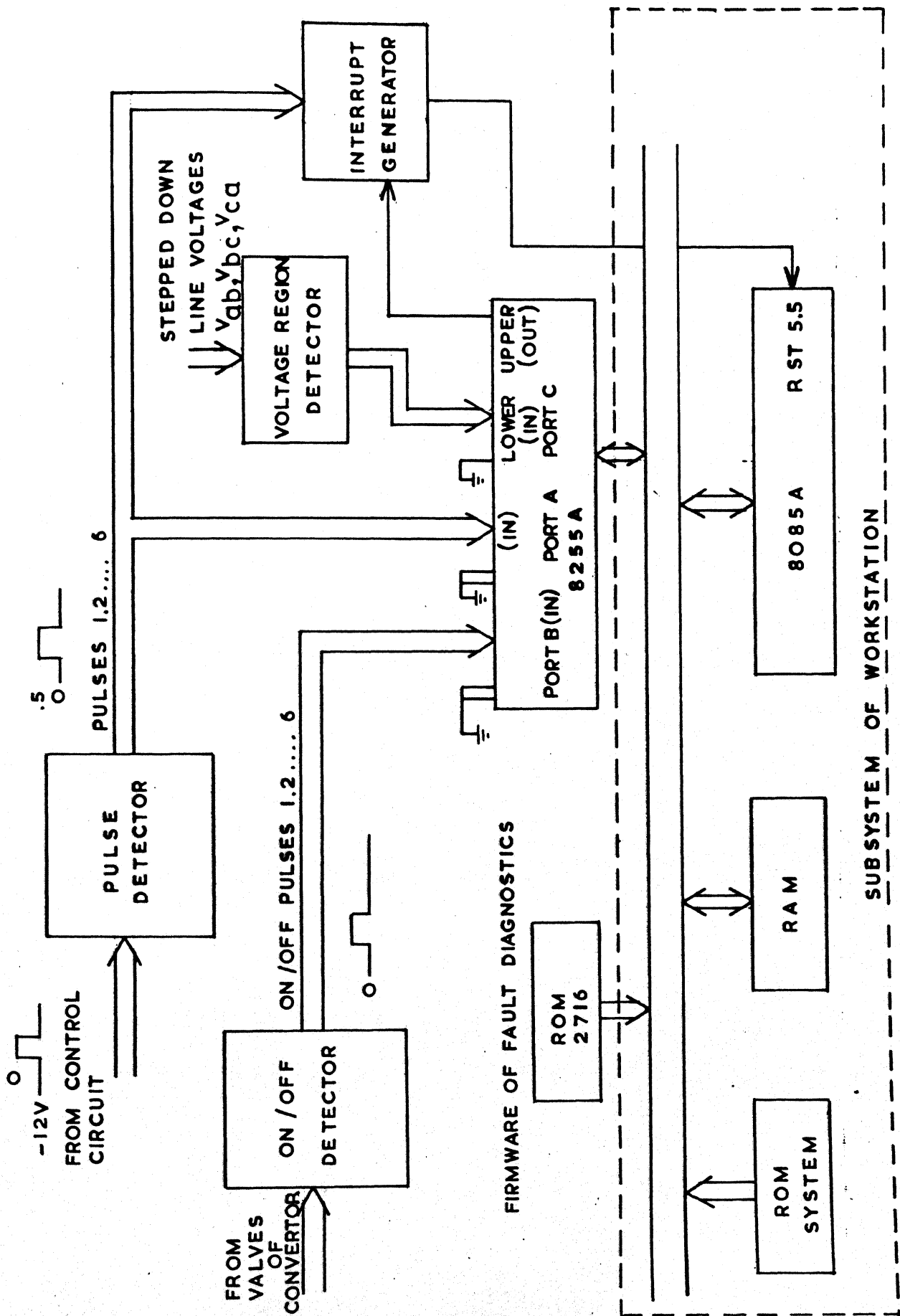


FIG.3.7 HARDWARE REALISATION OF THE SYSTEM (SHOWS THE INTERFACE TO WORKSTATION)

input port A of 8255A. The three voltage region signals from the voltage region detector are fed to the input port C. The six ON/OFF valve status signals are fed to the input port B. The six firing pulse signals (P_1 to P_6) are also fed to the interrupt generator as shown in Fig. 3.8. Each rising edge of the pulse produces a low level RST 5.5 interrupt, which is reset to high by output port C after interrupting to fault detection routine. The 8085A is connected through a bus to the workstation.

The workstation used is based on Intel's 8085 μP , developed at I.I.T. Kanpur. The workstation comprises of mainly the memory part and 8085A μP . The memory part consists of a ROM where the fault diagnostic software is installed. The system RAM is used for the variables of the software. The system ROM consists of resident system software which manages the workstation and provides environment suitable for the execution of detection routine.

3.5 CONCLUSIONS

This chapter describes the development of the various detection circuits to derive information regarding pulse regions, voltage regions and ON/OFF status of the valves.

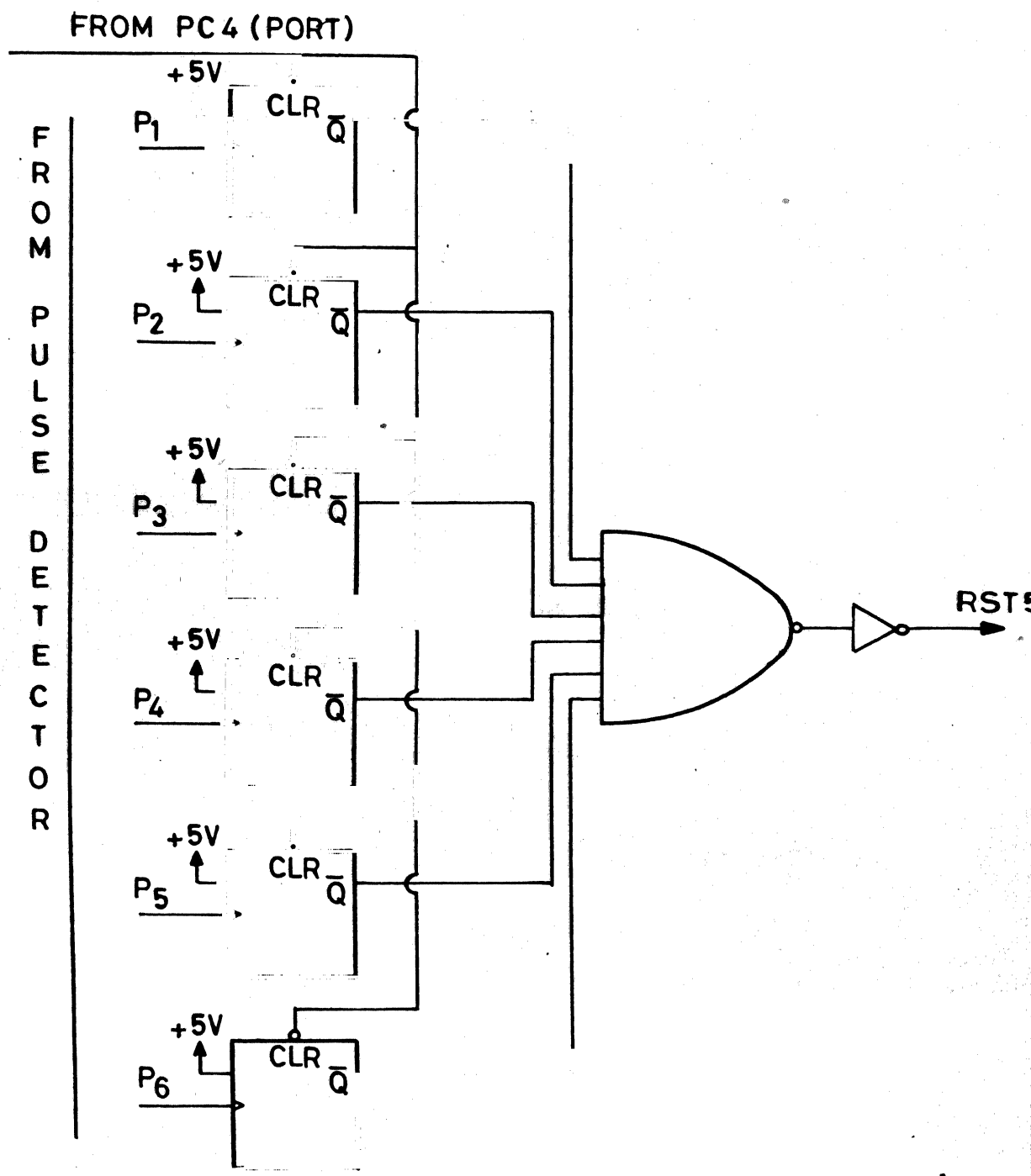


FIG. 3.8 INTERRUPT GENERATOR

The interconnection of various detection circuits to the microprocessor workstation is also discussed. This information is used as input to the fault detection software, the realisation of which is described in the next chapter.

CHAPTER 4

SOFTWARE REALISATION OF FAULT DETECTION SCHEME

This chapter explains the software developed to realise the fault detection scheme and experimental results carried out on the scheme. Of the various faults described in Chapter 2 only the detection of misfire and single commutation failure have been implemented.

Software realised is explained under the following three subsections.

- 4.1 Main program,
- 4.2 Normal converter status routine,
- 4.3 Fault detection routine.

4.1 MAIN PROGRAM

The flow chart of the main program is given in Fig. 4.1 and assembly language version is given in Appendix B. This program initialises all input and output ports, software timer and assigns program constants. After initialisation the fault detection process is synchronised to the control

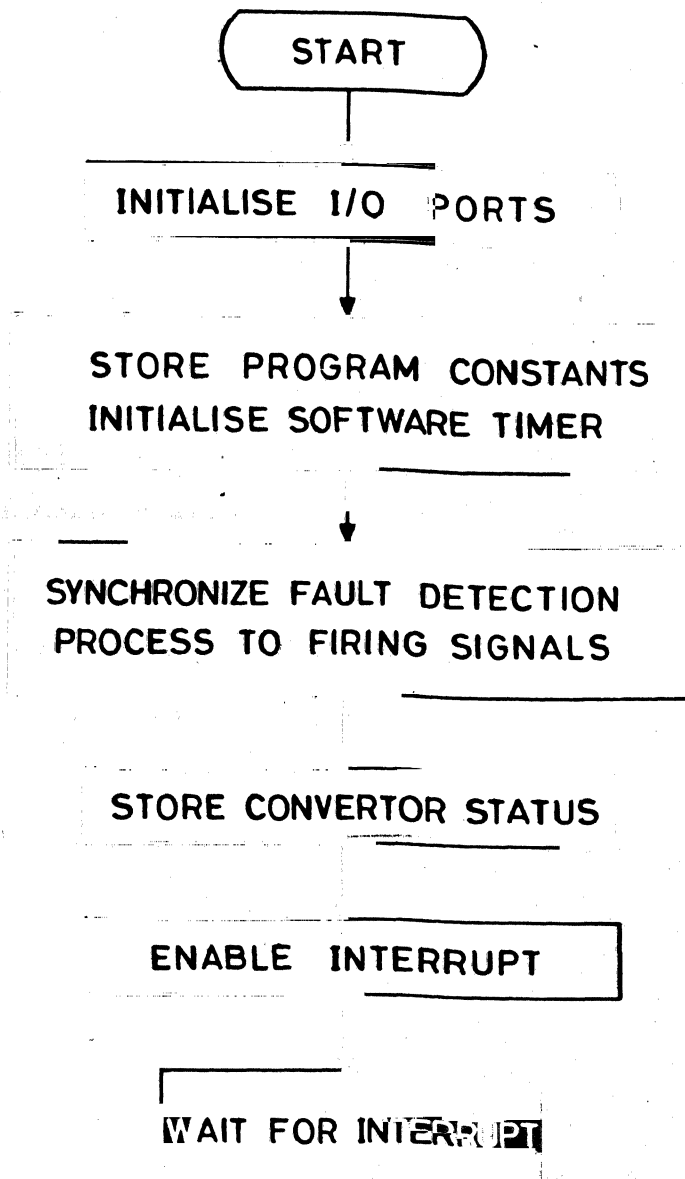


FIG.4.1 FLOW CHART OF MAIN PROGRAM.

firing signals and the converter's pulse, voltage and valve ON/OFF status is stored. Then the interrupt is enabled. Finally it enters a wait loop and stays in that state until interrupted either for fault detection or for display of normal status of converter.

4.2 NORMAL CONVERTER STATUS DISPLAY ROUTINE

The flow chart of this program is given in Fig. 4.2. Upon receiving the timer interrupt from the software counter which occurs every one minute, the processor makes a copy of conduction status of the converter existing in the previous one cycle. This information is stored in a table in the memory. The copying procedure enables to completely display the converter status at a particular time instant under consideration. Instead of copying, if the converter status is directly displayed then the hardware interrupt for fault detection may effect the display contents during the time of display. After making this copy a message is sent to the monitor that the conduction is normal. Then the converter status is displayed after decoding it in a friendly way. The firing angle is displayed whether it is in 0-60, 60-120 or 120-180 degree range. In the last step the processor presets the software timer and returns to the wait state of the main program. The normal conduction

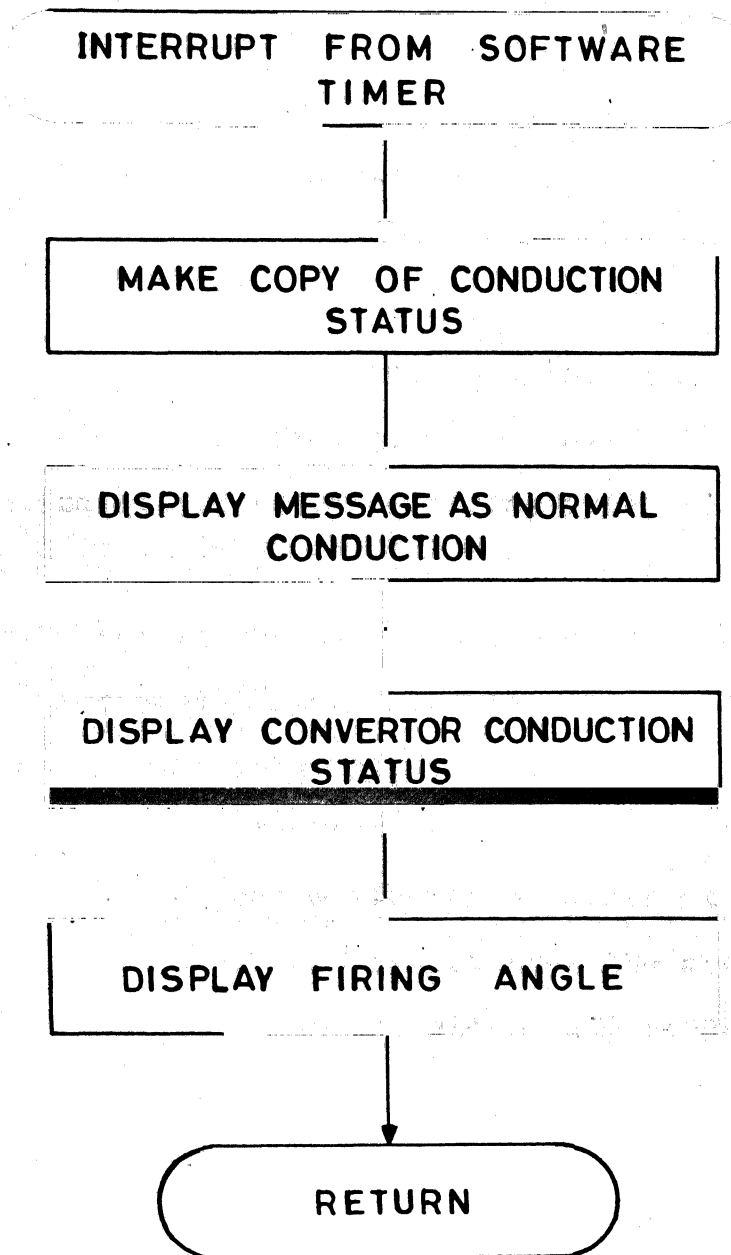


FIG. 4.2 FLOWCHART OF NORMAL CONVERTOR STATUS ROUTINE.

display consists of information on the conducting valves during different pulse regions and corresponding voltage regions in the form shown in Table 4.1. Also the range of the firing angle is displayed.

4.3 FAULT DETECTION ROUTINE

The flow chart to implement the fault diagnostic scheme is given in Fig. 4.3. The RST 5.5 interrupt generation at the start of firing pulse calls this routine. The processor after executing this routine returns back to the wait loop in the main program before the occurrence of next firing pulse interrupt. This routine, therefore, is executed in each pulse region once. Immediately after entering this routine the processor scans the firing pulse status and finds out whether the interrupt is caused by the expected pulse, if this is not true the processor displays the fault as firing pulse failure and stops execution. If the check is true, i.e., the occurrence of normal firing pulse interrupt the valve ON/OFF state is read and compared with expected normal three valve conduction pattern which occurs during commutation under normal conditions. The normal conduction status needed is accessed from the memory. If true then the processor takes note of this and waits for commutation of valves to be completed such that

Table 4.1 The normal conduction display

Port contents			Between zero crossing of thyristors	Firing pulses present for thyristors	Thyristors conducting
C	A	B			
05	03	03	6 and 1	6 and 5	6 and 5
04	21	21	1 and 2	6 and 1	6 and 1
06	30	30	2 and 3	2 and 1	2 and 1
02	18	18	3 and 4	3 and 2	3 and 2
03	0C	0C	4 and 5	4 and 3	4 and 3
01	06	06	5 and 6	5 and 4	5 and 4

Angle of advance is between 0 and 60

Normal conduction

Fault

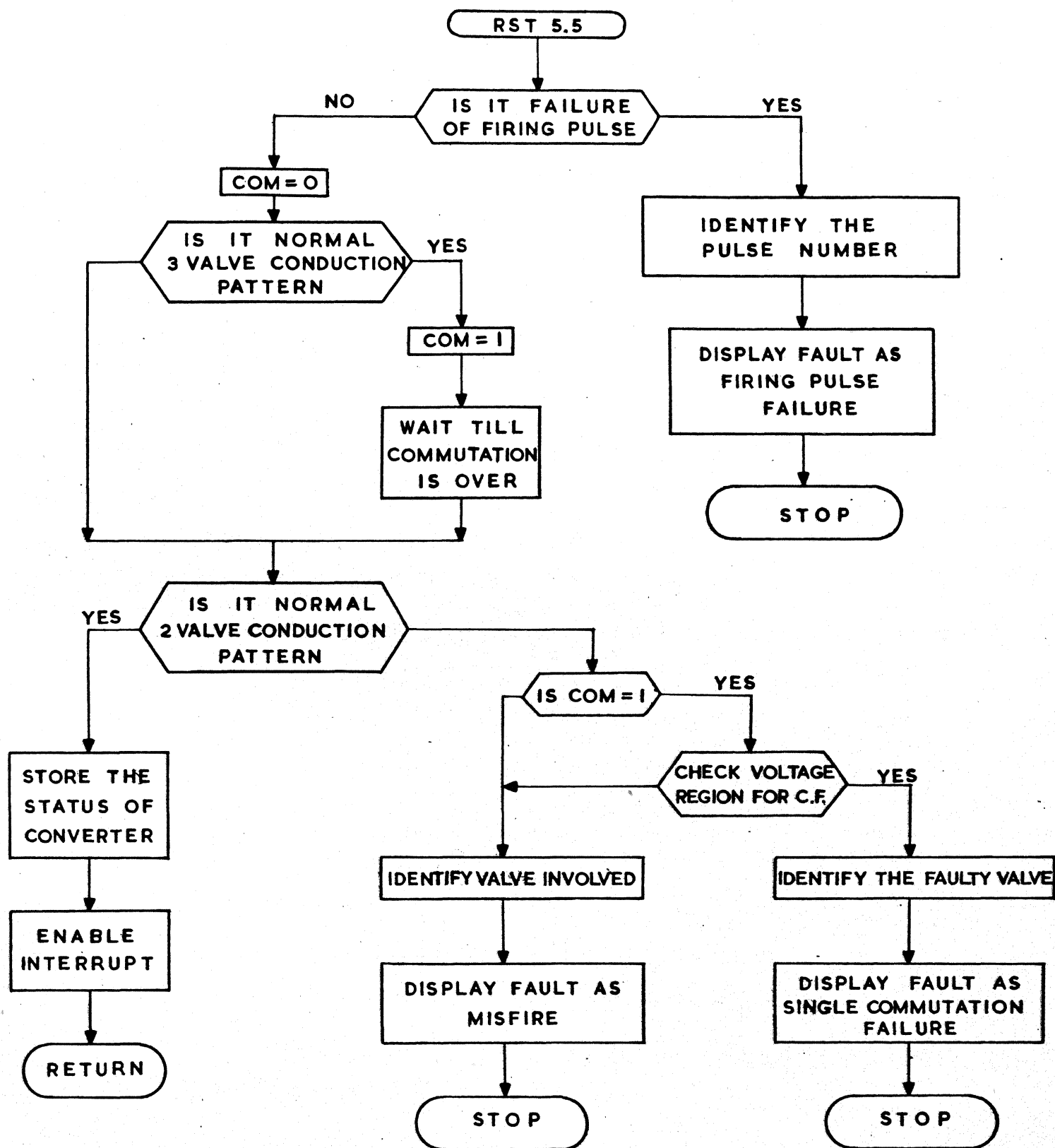


FIG. 4.3 FLOW CHART OF FAULT DETECTION ROUTINE

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Acc. No. A109362

two valve conduction comes into being. The ON/OFF status is again read and compared to check whether it is a normal two valve conduction pattern. If the pattern is normal the processor stores the present converter status and enables the interrupt before returning to the main program. In case the above check for normal two valve conduction fails, the conduction state is considered abnormal and the processor reads the voltage region and checks with the corresponding voltage region (ref. Section 2.3) for occurrence of the commutation failure. If the check is positive the faulty valve involved is identified and message is sent to monitor as commutation failure of the incoming valve. If the check turns out to be negative then the fault is displayed as misfire of that particular valve. In either case the processor stops the execution of the fault detection routine after displaying messages. This is done as the objective is to detect only the first occurrence of the fault. In case the fault detection routine is allowed to continue execution it would be necessary to include the development into subsequent faults.

The misfire of the valve as considered in the fault diagnostic routine can be due to anyone of the following reasons.

1. The firing pulse is generated by the converter control system but it is either insufficient or has not reached the valve.
2. The proper firing pulse although has reached the valve, the valve fails to fire due to some internal problem with the valve.

In either case, in a given pulse region, the flag 'COM' (Fig. 4.3) will not be equal to 1 due to the failure of the valve to fire. This denotes the misfire of a particular valve as the conduction pattern will not be normal with reference to the pulse region under consideration.

In Fig. 4.3 it can be seen that a fault is displayed as a misfire even when 'COM' = 1. This situation actually refers to a premature cessation of valve conduction. This is called arcquenching which takes place mainly in case of mercury arc valves but not for thyristor valves.

4.4 EXPERIMENTAL SET UP AND RESULTS

The software details of the fault diagnostic scheme described in the previous section is implemented on 8085 μ P workstation built at I.I.T. Kanpur. The feature of the workstation are given in Appendix A. The hardware detection circuits are appropriately interfaced using I/O ports and

and interrupt generator which are in turn connected to the buffered bus of the workstation.

For the hardware detection circuit, the necessary inputs, viz., three line voltages, valve currents and firing pulses are provided from the H.V.D.C. simulator. The simulator is a physical scaled down model (100 VDC, 1 Amp) of a two terminal d.c. link. The simulator is operated under manual control, i.e., with fixed firing angles at both the terminals.

The input and output of the ON/OFF detection circuit, pulse detector and voltage region detector are shown in Figs. 4.4 to 4.6. In Fig. 4.4, the trace (a) shows the normal d.c. voltage waveform across the inverter terminal. The voltage across valve 1 and the current through valve 1 during normal inverter operation are shown in traces (b) and (c) respectively. The input to the ON/OFF detection circuit for valve 1 is the valve current (trace (c)) and the corresponding output is shown in trace (d).

In Fig. 4.5, trace (a) shows the sinusoidal commutation voltage V_{ac} for valve 1. Trace (b) shows the valve 1 firing pulse as obtained from the firing pulse generator of the simulator, it is evident that the firing angle of valve 1 is around 160° . For the pulse detection circuit

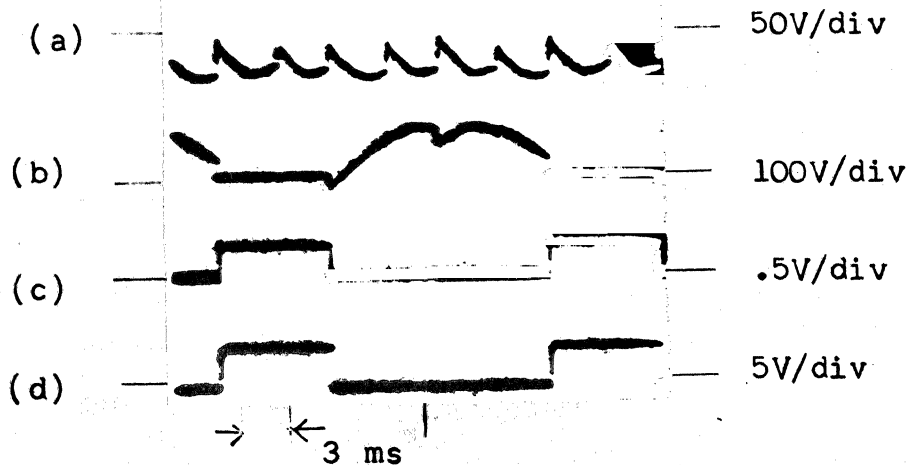


Fig. 4.4 Oscilloscope waveforms for ON/OFF detection circuit

- (a) Inverter dc voltage
- (b) Voltage across valve 1
- (c) Valve 1 current
- (d) Output of ON/OFF detector

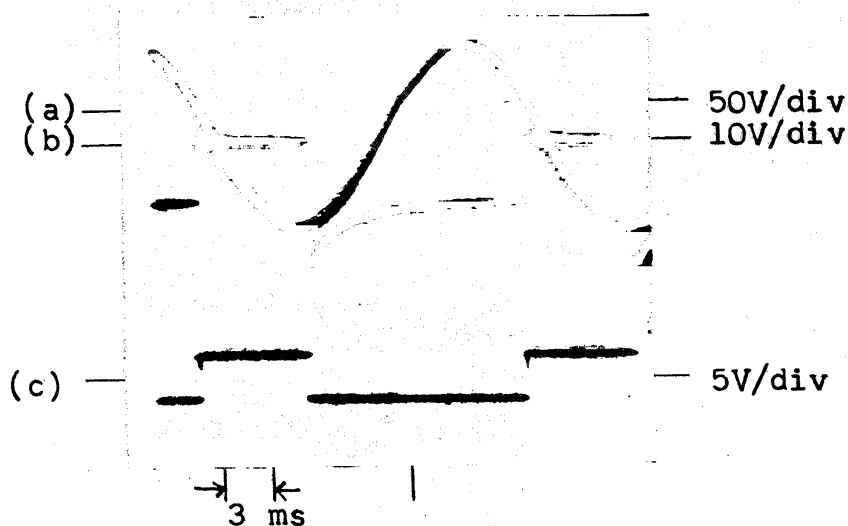


Fig. 4.5 Oscilloscope waveforms for pulse detection circuit

- (a) Commutation voltage of valve 1 V_{ac}
- (b) Firing pulse input
- (c) Pulse detected output

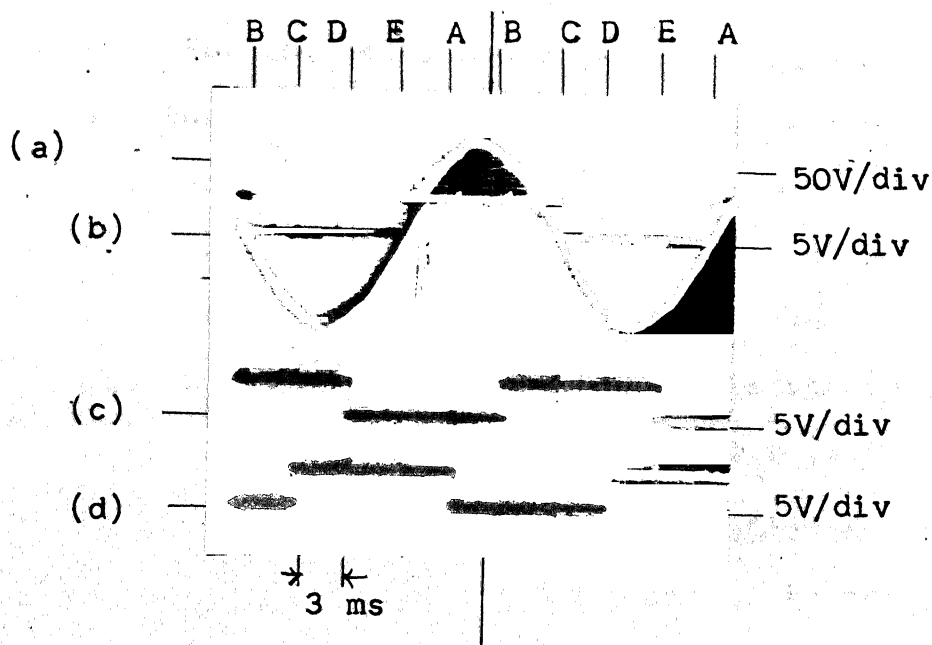


Fig. 4.6 Oscillograms for voltage detector

(a) Line voltage V_{ab}

(b) Digitized output V_{ab}

(c) Digitized output V_{bc}

(d) Digitized output V_{ca}

of valve 1 the input applied is the firing pulse trace (b) and the corresponding output obtained is shown in trace (c).

For the detection of voltage region the input required are three phase a.c. voltages. In Fig. 4.6, trace (a) shows one such input (V_{ab}) for which the output is shown in trace (b). Corresponding to the input voltages V_{bc} and V_{ca} the outputs are shown in traces (c) and (d). The superposition of these three outputs (traces (b), (c) and (d)) determines the voltage region A to F (refer Fig. 3.5).

The outputs of the various detection circuits are appropriately used for determining the normal conduction status of the converter and the diagnostics of the converter fault. The information regarding normal conduction status of the converter over one a.c. cycle displayed on the monitor of the workstation at regular time intervals (say every 1 minute). This information which is important from the operator's point of view, comprises of the details regarding the presence of firing pulses, the conducting thyristors and the range of firing angle. A sample display of the normal conduction status of a rectifier terminal on the monitor screen is shown in Fig. 4.7.

The occurrence and detection of a misfire of valve 1 at the rectifier terminal is illustrated in Fig. 4.8. The

NORMAL CONDUCTION			BETWEEN ZERO CROSSING OF THYRISTORS	FIRING PULSES PRESENT FOR THYRISTORS	THYRISTORS CONDUCTING
PORT CONTENTS					
C	A	B			
05	03	03	6 AND 1	6 AND 5	6 AND 5
04	21	21	1 AND 2	6 AND 1	6 AND 1
06	30	30	2 AND 3	2 AND 1	2 AND 1
02	18	18	3 AND 4	3 AND 2	3 AND 2
03	0C	0C	4 AND 5	4 AND 3	4 AND 3
01	06	06	5 AND 6	5 AND 4	5 AND 4
ANGLE OF ADVANCE IS BETWEEN 0 AND 60					
NORMAL CONDUCTION					

FAULT					

Fig. 4.7 Conduction status display on the monitor under normal condition

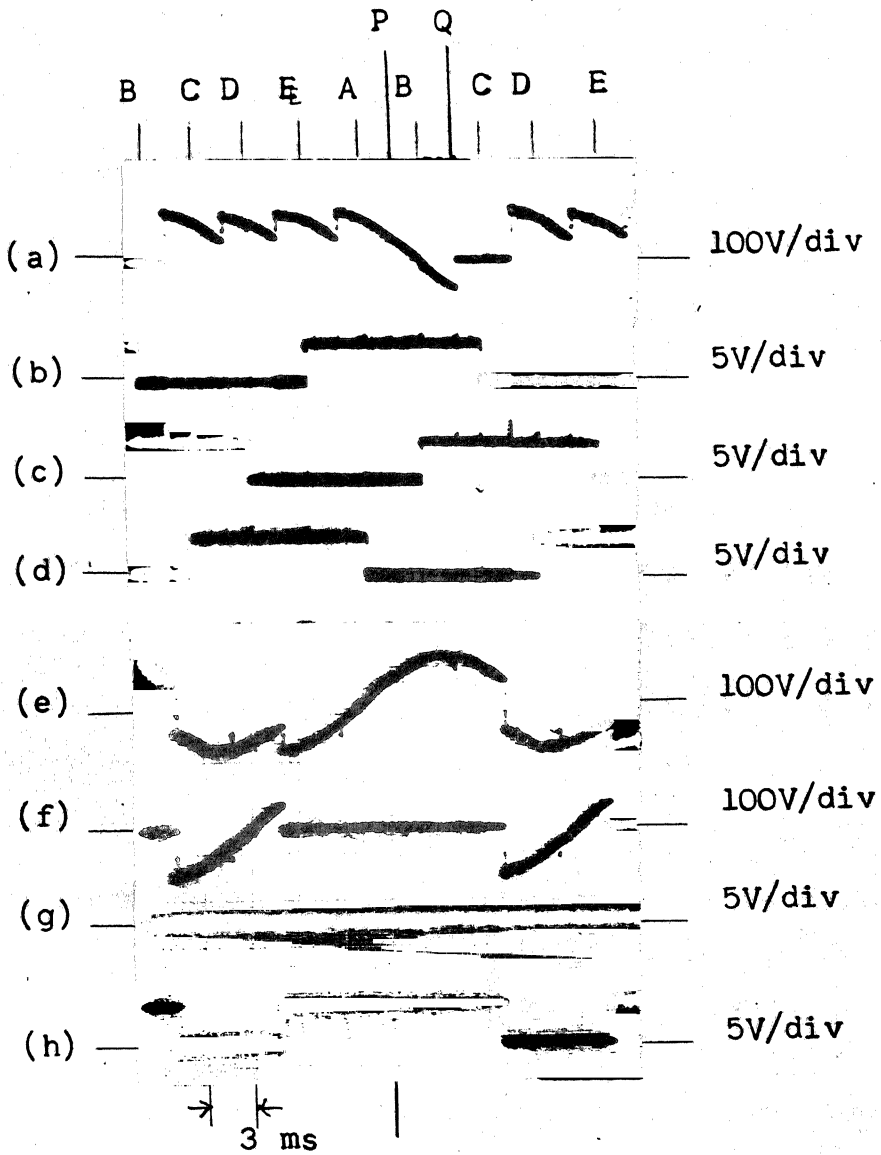


Fig. 4.8 Oscillograms for misfire of valve 1
 (a) DC voltage across converter
 (b), (c) and (d) Voltage region signals
 (e) Voltage across valve 1
 (f) Voltage across valve 5
 (g) ON/OFF signal of valve 1
 (h) ON/OFF signal of valve 5

misfire of valve 1 which is simulated by creating an open circuit in the arm of valve 1, occurs at a instant P. Following which the output d.c. voltage is of the form shown in trace (a) as the valves 5 and 6 continue to conduct (in the absence of valve 1) till valve 2 ignites (at instant Q) and the d.c. voltage collapses to zero. The valid voltage region in which misfire of valve 1 can take place is A E (ref. to Table 2.1). This fact is established through traces (b), (c) and (d), which shows that instant P at which misfire of valve 1 occurs is in AB (which is a portion of the valid region AE). Following the misfire the voltage across valve 1 and valve 5 is shown in traces (e) and (f). The trace (g) which is the output of valve 1 ON/OFF detection circuit shows that current through valve 1 is zero whereas the trace (h) shows that valve 5 conducts for approximately 240° .

The fault diagnostic scheme has also been successfully tested for the detection of single commutation failure which is made to occur at the inverter terminal of the H.V.D.C. simulator by increasing the inverter firing angle to around 175° . It has not been possible to reproduce the various oscillograms under the condition of commutation failure as the protection unit on the H.V.D.C. simulator operates due to excessive d.c. current. This leads to the shutdown of the system.

4.5 CONCLUSIONS

This chapter describes the software implementation of the fault diagnostic scheme on the μ P workstation. The effectiveness of fault detection scheme is illustrated experimentally through simulation and detection of the misfire and single commutation failure.

CHAPTER 5

CONCLUSIONS

The diagnosis of a converter fault is important to ensure reliable and satisfactory operation of a H.V.D.C. system. Also, an effective diagnostic system can lead to reduction in repair time, better maintenance and high availability of the d.c. system. The faults in H.V.D.C. converters can occur due to internal problems or external causes. Some of the commonly encountered converter faults/maloperation are arcbreak, arcthrough, arcquenching, misfire and commutation failure. Out of these, in thyristor converters, the last two are quite frequent.

The various converter faults/maloperation leads to an abnormal conduction pattern. Since a converter valve can begin conduction only when it is forward biased and the firing is present, the various conduction sequences, which may arise due to fault/maloperation, can be related in time to the a.c. voltage waveform and firing pulses. A detailed investigation of the converter logic behaviour during normal and abnormal conditions is reported in [1]. The analysis

illustrates that each of the maloperation have a unique combination of the valve conduction pattern and governing time zones which are bounded by the firing pulses and the voltage zero crossings of the a.c. supply. Thus, the information regarding the converter valve ON/OFF status, firing pulse region and voltage regions forms a convenient basis for the detection of converter faults as discussed in Chapter 2. The hardware details for deriving these information based on the signals obtained from the H.V.D.C. simulator are described in Chapter 3. This chapter also describes the interface of the outputs from ON/OFF detection circuit firing pulse detector and voltage region detector with the μP workstation. The software algorithms for identifying a particular fault and the valve involved therein is discussed in Chapter 4. In the absence of the converter fault, the diagnostic scheme provides a display of the converter normal conduction status at regular time intervals which is important for system operator. The fault diagnostic system has been tested for the detection of misfire and single commutation failure. Although at present, only the first occurrence of these two faults has been detected, the algorithm is extremely flexible to incorporate detection of other converter faults.

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3. Murthy, Dubey, 'Fault diagnosis of three-phase thyristor converters using μP ', IEEE Trans. on Industry Applications, vol. IA-20, No.6, Nov/Dec. 1984.
4. J. Arrillaga, H. Hisha, 'Fast ON/OFF detection of silicon-controlled rectifiers and its influence on converter controllability', IEEE Trans. on Ind. Elect. and Control Instrumentation, vol. IECI-26, No.1, Feb. 1979.
5. Kimbark, Direct current transmission.

APPENDIX A

HARDWARE DETAILS

Workstation Interfacing

The relevant pins of the Workstation processor have been brought out for direct external interfacing for the users, after being properly buffered. The pin- outs are briefly described below:

SL. NO	PIN NO.	NAME	DESCRIPTION
1	17 to 2 (TOP)	A0-A15	This is the address Bus of the 8085A CPU. The lower order address bus which is multiplexed with the data bus at the 8085A output is brought out after being demultiplexed.
2	10 to 3 (BOTTOM)	D0-D7	This is the data bus of 8085A which is brought out through buffers.
3	12 (BOTTOM)	\overline{RD}	This is the signal by which data is read from memory/IO devices into the CPU. It is active at the falling edge of the signal.
4	13 (BOTTOM)	\overline{WR}	This is the signal by which data is written into the memory/IO devices from the CPU. It is active at the rising edge of the signal.
5	11 (BOTTOM)	IO/\overline{M}	This signal distinguishes between an I/O & a memory operation. It is low when a memory read/write cycle is being performed and high when a I/O read/write cycle is being performed.

L. NO	PIN NO.	NAME	DESCRIPTION
6	16 ,17 (BOTTOM)	S0,S1	These two control lines indicate the type of current bus cycle: 1)Halt(S0S1=00) 2)Read(S0S1=01) 3)Write(S0S1=10) 4)Opcode Fetch(S0S1=11)
7	15 (BOTTOM)	RDY	This is an asynchronous handshaking input signal for slow memory devices. This signal is normally kept high. When the CPU generates a bus cycle for a slow memory device, this signal may be negated(low) by external logic to make the CPU go into wait states,thus prolonging the bus cycle indefinitely.
8	19 to 21 (BOTTOM)	<u>5.5</u> , <u>6.5</u> , <u>7.5</u>	These are the three vector interrupt lines of the 8085A being given to the user.The 7.5 has the highest priority and is edge sensitive, while the 6.5 and 5.5 are level sensitive and have decreasing priority levels. All three interrupts are pulled up and have negative logic (applied through inverting buffers).
9	2 (BOTTOM)	<u>BDIS</u>	This is a line which, when asserted, disables the internal CPU bus. This is required when the user wants to have an external bus master (e.g. a DMA controller).
10	14 (BOTTOM)	<u>RES IN</u>	This input is brought out for the user to give an external Reset to the CPU.
11	19 (TOP)	RES OUT	This is the Reset Out from the CPU for resetting external devices.

SL. NO	PIN NO.	NAME	DESCRIPTION
12	20,21 (TOP)	HOLD, HLDA	These are the two lines to force and monitor the HOLD state.
13	18 (TOP)	CLK(3 MHZ.)	This is the Clock Output of the CPU, brought out for use by external devices.
14	1&22 (Both TOP & BOTTOM)	+5V & GND.	The power supply pins, brought out for external connection.

Following table gives a complete description of the Memory and I/O Maps of the Workstation peripherals:

CARD	MEMORY/ IO	DEVICE	ADDRESS
CPU CARD	M	EPROM(4X2732A)	0000-3FFF
	M	USER'S RAM (12X2114)	4000-57FF
	M	SYSTEM RAM (4X2114)	5800-5FFF
	I/O	USART (8251A)	F8-F9
	I/O	TIMER (8253)	FC-FF
I/O CARD	I/O	TIMER (8253)	A0 - A7
	I/O	DAC (8255)	B8 - BF
	I/O	USART(8251)	B0 - B7

APPENDIX B

THE FOLLOWING ASSEMBLY LANGUAGE
PROGRAM(INTEL 8085A) IS DEVELOPED
TO DETECT VARIOUS FAULTS IN A 6-
PULSE BRIDGE CONVERTER

THE FAULTS DETECTED ARE
MISFIRE OF VALVE
SINGLE COMMUTATION FAILURE OF
VALVE

8255 IS PROGRAMMED IN MODE 0

PORT	I/O	ADDRESS
A	INPUT	C0H
B	INPUT	C1H
C(LOWER)	INPUT	C2H
C(UPPER)	OUTPUT	C2H

LOC	OBJ	LINE	SOURCE STATEMENT
0093		1	CM55 EQU 93H
8000		2	CPY EQU 8000H
8400		3	ORG 8400H
8400	3E93	4	MAI: MVI A, 093H
8402	D3C3	5	OUT 0C3H
8404	3E0E	6	MVI A, 0EH
8406	30	7	SIM
8407	2A0A40	8	LHLD 400AH
840A	220C40	9	SHLD 400CH
840D	DBC0	10	BSY1: IN 0C0H
840F	2F	11	CMA
8410	FE06	12	CFI 06H
8412	C20D84	13	JNZ BSY1
8415	DBC0	14	BSY2: IN 0C0H
8417	2F	15	CMA
8418	FE03	16	CFI 03H
841A	C41E04	17	JNZ BSY2

841D 320040	18 STA 4000H
8420 3EFF	19 MVI A, 0FFH
8422 D3C2	20 OUT 0C2H
8424 3E00	21 MVI A, 00
8426 D3C2	22 OUT 0C2H
8428 2A0C40	23 LOOP: LHLD 400CH
842B 7C	24 MOV A, H
842C FE00	25 CPI 00H
842E FC0080	26 CM CPY
8431 C32884	27 JMP LOOP
8400	28 END MAI

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS

BSY1	A 840D	BSY2	A 8415	CM55	A 0093
CPY	A 8000	LOOP	A 8428	MAI	A 8400

 THE FOLLOWING 8085 ASSEMBLY LANGUAGE
 ROUTINE DISPLAYS THE STATUS OF CONVERTER
 IN PREVIOUS ONE CYCLE OF A.C VOLTAGE
 WHEN CALLED.

LOC	OBJ	LINE	SOURCE STATEMENT
0267		1	PRINT EQU 0267H
02B7		2	CRLF EQU 02B7H
02C4		3	TWOSP EQU 02C4H
0438		4	PNTMS EQU 0438H
03BD		5	BIHEX EQU 03BDH
8000		6	CBASE EQU 8000H
8000		7	ORG CBASE
8000 2A0140		8	CPY: LHLD 4001H
8003 3A0540		9	LDA 4005H
8006 4F		10	MOV C, A
8007 7E		11	RCPY: MOV A, M
8008 FE05		12	CPI 05H
800A CA1D80		13	JZ CP1
800D 2C		14	INR L
800E 2C		15	INR L
800F 2C		16	INR L
8010 0D		17	DCR C
8011 0D		18	DCR C
8012 0D		19	DCR C
8013 C20780		20	JNZ RCPY
8016 2A0A40		21	LHLD 400AH
8019 220C40		22	SHLD 400CH
801C C9		23	RET ; FINDS THE ADDR OF VOL REGION 05
801D EB		24	CP1: XCHG
801E 2A0640		25	LHLD 4006H
8021 EB		26	XCHG
8022 3A0540		27	LDA 4005H
8025 4F		28	MOV C, A
8026 3A0340		29	LDA 4003H
8029 47		30	MOV B, A
802A 04		31	INR B
802B 7E		32	RCP1: MOV A, M
802C EB		33	XCHG
802D 77		34	MOV M, A
802E EB		35	XCHG
802F 23		36	INX H
8030 13		37	INX D
8031 0D		38	DCR C
8032 CA4180		39	JZ ECP1
8035 7D		40	MOV A, L
8036 B8		41	CMP B
8037 C22B80		42	JNZ RCP1
803A 2A0140		43	LHLD 4001H

803D C32B80	44 JMP RCP1	; MAKES A COPY OF STATUS TABLE
8040 00	45 NOP	
8041 CD4C80	46 ECP1:CALL DSP	; DISPLAY THE DATA IN USER FRIE
8044 2A0940	47 LHLD 4009H	
8047 220B44	48 SHLD 440BH	; INITIATE THE COUNTER
804A C9	49 RET	; END OF MAIN OF DISPLAY
804E 00	50 NOP	
804C CD9681	51 DSP:CALL DIND	; DISPLAY "NORM COND"
804F 2A1840	52 LHLD 4018H	
8052 CD7981	53 CALL DIHE	; DISPLAY THE HEADING
8055 2A0640	54 LHLD 4006H	

8058 3A0540	55 LDA 4005H	
805B 5F	56 MOV E, A	
805C 46	57 RDSP: MOV B, M	
805D 23	58 INX H	
805E 1D	59 DCR E	
805F 4E	60 MOV C, M	
8060 23	61 INX H	
8061 1D	62 DCR E	
8062 56	63 MOV D, M	
8063 CDE380	64 CALL DIDA	
8066 23	65 INX H	
8067 1D	66 DCR E	
8069 C25080	67 JNZ RDSP	
806B 2A0640	68 LHLD 4006H	
806E 46	69 MOV B, M	
806F 23	70 INX H	
8070 4E	71 MOV C, M	
8071 CD1A81	72 CALL DIF	; DISPLAY FIRING ANGLE
8074 CD9681	73 CALL DINO	; DISPLAY "NOR COND"
8077 CDA681	74 CALL DIFT	; DISPLAY MESSAGE "FAULT"
807A C9	75 RET	
807B 00	76 NOP	
807C 3E20	77 SPDI: MVI A, 20H	
807E CD6702	78 RSP: CALL PRINT	
8081 1D	79 DCR E	
8082 C27E80	80 JNZ RSP	; DISPLAYS (E) NO OF BLANK
8085 C9	81 RET	
8086 00	82 NOP	
8087 C5	83 DEVOL: PUSH B	
8088 2A0F40	84 LHLD 400FH	
808B 7D	85 MOV A, L	
808C E6F0	86 ANI 0F0H	
808E B0	87 ORA B	
808F 6F	88 MOV L, A	
8090 7E	89 MOV A, M	
8091 FE06	90 CPI 06H	
8093 CAAB80	91 JZ VOL6	
8096 F630	92 ORI 30H	
8098 47	93 MOV B, A	
8099 CD6702	94 CALL PRINT	; DISPLAY THE TRND
809C C5	95 PUSH B	
809D 012940	96 LXI B, 4029H	
80A0 CD3804	97 CALL PNTMS	
80A3 C1	98 POP B	; DISPLAYS " AND "
80A4 78	99 MOV A, B	
80A5 3C	100 INR A	
80A6 CD6702	101 CALL PRINT	
80A9 C1	102 POP B	
80AA C9	103 RET	
80AB F630	104 VOL6: ORI 30H	
80AD CD6702	105 CALL PRINT	
80B0 012940	106 LXI B, 4029H	
80B3 CD3804	107 CALL PNTMS	
80B6 3E31	108 MVI A, 31H	
80B8 CD6702	109 CALL PRINT	

80BB C1	110 POP B	
80BC C9	111 RET	
80BD 00	112 NOP	
80BE 79	113 DECFU: MOV A, C	
80C1 37	115 STC	
80C2 3F	116 CMC	
80C3 05	117 RDE: DCR B	
80C4 0F	118 RRC	
80C5 D2C380	119 JNC RDE	
80C8 F5	120 PUSH PSW	
80C9 C5	121 PUSH B	
80CA 78	122 MOV A, B	
80CB CD6702	123 CALL FRINT ; PRINT TR(B)3	
80CE 012940	124 LXI B, 4029H	
80D1 CD3804	125 CALL PNTMS	
80D4 C1	126 POP B	
80D5 F1	127 POP PSW ; PRINT " AND "3	
80D6 37	128 STC	
80D7 3F	129 CMC	
80D8 05	130 RDE1: DCR B	
80D9 0F	131 RRC	
80DA D2D880	132 JNC RDE1	
80DB 78	133 MOV A, B	
80DE CD6702	134 CALL PRINT	
80E1 C9	135 RET	
80E2 00	136 NOP	
80E3 D5	137 DIDA: PUSH D	
80E4 E5	138 PUSH H	
80E5 78	139 MOV A, B	; DISPLAY VOL3
80E6 CDBD03	140 CALL BIHEX	
80E7 CDC402	141 CALL TWOSP	
80EC 79	142 MOV A, C	; DISPLAY PULSE3
80ED CDBD03	143 CALL BIHEX	
80F0 CDC402	144 CALL TWOSP	
80F3 7A	145 MOV A, D	; DISPLAY ON/OFF3
80F4 CDBD03	146 CALL BIHEX	
80F7 1E06	147 MVI E, 06H	
80F9 CD7C80	148 CALL SPDI	; DISPLAY DECODED VOL3
80FC CD8780	149 CALL DEVOL	
80FF 1E08	150 MVI E, 08H	
8101 CD7C80	151 CALL SPDI	; DISPLAY DECODED PULSE3
8104 CDBE80	152 CALL DECFU	
8107 1E09	153 MVI E, 09H	
8109 CD7C80	154 CALL SPDI	
810C 4A	155 MOV C, D	; DISPLAY DECODED ON/OFF3
810D CDBE80	156 CALL DECFU	
8110 CDB702	157 CALL CRLF	
8113 CDB702	158 CALL CRLF	
8116 E1	159 POP H	
8117 D1	160 POP D	
8118 C9	161 RET	
8119 00	162 NOP	
811A C5	163 DIF: PUSH B	
811B 015640	164 LXI B, 4056H	

LOC	OBJ	LINE	SOURCE STATEMENT
811E	CD3804	165	CALL PNTMS
8121	C1	166	POP B ;PRINT "FIRING ANGLE-----"3
8122	79	167	MOV A,C
8123	FE03	168	CPI 03H
8125	CA4B81	169	JZ DIF0
8128	FE06	170	CPI 06H
812A	CA5F81	171	JZ DIF6
812D	3E31	172	MVI A,31H
812F	CD6702	173	CALL PRINT
8132	3E20	174	MVI A,20H
8134	CDBD03	175	CALL BIHEX
8137	012940	176	LXI B,4029H
813A	CD3804	177	CALL PNTMS
813D	3E31	178	MVI A,31H
813F	CD6702	179	CALL PRINT
8142	3E80	180	MVI A,80H
8144	CIBD03	181	CALL BIHEX ;DISPLAY" 120 AND 180"3
8147	CDB702	182	CALL CRLF
814A	C9	183	RET
814B	3E30	184	DIF0:MVI A,30H
814D	CD6702	185	CALL PRINT
8150	012940	186	LXI B,4029H
8153	CD3804	187	CALL PNTMS
8156	3E60	188	MVI A,60H
8158	CIBD03	189	CALL BIHEX ;DISPLAYS "0 AND 60"3
815B	CDB702	190	CALL CRLF
815E	C9	191	RET
815F	3E60	192	DIF6:MVI A,60H
8161	CDBD03	193	CALL BIHEX
8164	012940	194	LXI B,4029H
8167	CD3804	195	CALL PNTMS
816A	3E31	196	MVI A,31H
816C	CD6702	197	CALL PRINT
816F	3E20	198	MVI A,20H
8171	CDBD03	199	CALL BIHEX ;DISPLAYS "60 AND 120"3
8174	CDB702	200	CALL CRLF
8177	C9	201	RET
8178	00	202	NOP
8179	3A1A40	203	DIHE:LDA 401AH
817C	5F	204	MOV E,A
817D	7E	205	ROT:MOV A,M
817E	FE2A	206	CPI 2AH
8180	CA9181	207	JZ EDIH
8183	CD6702	208	CALL PRINT
8186	23	209	INX H
8187	1D	210	DCR E
8188	C27D81	211	JNZ ROT
818B	CDB702	212	CALL CRLF
818E	C37981	213	JMP DIHE
8191	CDB702	214	EDIH:CALL CRLF
8194	C9	215	RET
8195	00	216	NOP
8196	CDB702	217	DINO:CALL CRLF
8199	C5	218	PUSH B
819A	013240	219	LXI B,4032H

LOC	OBJ	LINE	SOURCE STATEMENT
819D	CD3804	220	CALL PNTMS
81A0	C1	221	POP B
81A1	CDB702	222	CALL CRLF
81A4	C9	223	RET
81A5	00	224	NOP
81A6	00	225	DIFT: NOP
81A7	CDB702	226	CALL CRLF
81AA	CDBE81	227	CALL DIA ; DISPLAYS 39H -----S3
81AD	012040	228	LXI B, 4020H
81E0	CD3804	229	CALL PNTMS ; DISPLAYS "FAULT"3
81E3	CDB702	230	CALL CRLF
81E6	CDBE81	231	CALL DIA ; DISPLAYS 39H -----S3
81E9	CDB702	232	CALL CRLF
81BC	C9	233	RET
81BD	00	234	NOP
81BE	3A1A40	235	DIA: LDA 401AH
81C1	5F	236	MOV E, A
81C2	3E2D	237	MVI A, 2DH
81C4	CD6702	238	RDIA: CALL PRINT
81C7	1D	239	DCR E
81C8	C2C481	240	JNZ RDIA
81CB	CDB702	241	CALL CRLF ; DISPLAYS 39H -----S3
81CE	C9	242	RET
81CF	00	243	NOP
81D0	00	244	NOP
81D1	00	245	NOP
81D2	00	246	NOP
81D3	00	247	NOP
81D4	00	248	NOP

RST 5.5 INERRUPT ROUTINE.
THE FOLLOWING ROUTINE IS CALLED
AT THE START OF EACH
FIRING PULSE. THIS ROUTINE CHECKS
FOR THE FAULTS.

81D8 3EFF	252 FAU: MVI A, OFFH
81DA D3C2	253 OUT OC2H
81DC F5	254 PUSH PSW
81DD C5	255 PUSH B
81DE D5	256 PUSH D
81DF E5	257 PUSH H
81E0 210040	258 LXI H, 4000H
81E3 46	259 MOV B, M
81E4 68	260 MOV L, B
81E5 4E	261 MOV C, M
81E6 69	262 MOV L, C
81E7 56	263 MOV D, M
81E8 00	264 NOP
81E9 79	265 MOV A, C
81EA 2F	266 CMA
81EB A2	267 ANA D
81EC 57	268 MOV D, A
81ED 00	269 NOP
81EE DBC0	270 IN OCOH
81F0 2F	271 CMA
81F1 A2	272 ANA D
81F2 C25582	273 JNZ FFAI
81F5 00	274 NOP

LOC	OBJ	LINE	SOURCE STATEMENT
81F6	78	275	MOV A, B
81F7	2F	276	CMA
81F8	A1	277	ANA C
81F9	57	278	MOV D, A
81FA	00	279	NOP
81FB	DBC0	280	LP1: IN OCOH
81FD	2F	281	CMA
81FE	A2	282	ANA D
81FF	CAFB81	283	JZ LP1
8202	00	284	NOP
8203	78	285	MOV A, B
8204	B1	286	ORA C
8205	5F	287	MOV E, A
8206	00	288	NOP
8207	0600	289	MVI B, 00H
8209	04	290	LP2: INR B
820A	DBC1	291	IN OC1H
820C	2F	292	CMA
820D	A3	293	ANA E
820E	E20982	294	JPO LP2
8211	00	295	NOP
8212	A2	296	ANA D
8213	CA6382	297	JZ TFCF
8216	00	298	NOP
8217	DBC0	299	IN OCOH
8219	2F	300	CMA
821A	320040	301	STA 4000H
821D	00	302	NOP
821E	2A1B40	303	LHLD 401BH
8221	DBC2	304	IN OC2H
8223	E607	305	ANI 07H
8225	77	306	MOV M, A
8226	2C	307	INR L
8227	DBC0	308	IN OCOH
8229	2F	309	CMA
822A	77	310	MOV M, A
822B	2C	311	INR L
822C	DBC1	312	IN OC1H
822E	2F	313	CMA
822F	77	314	MOV M, A
8230	3A0340	315	LDA 4003H
8233	47	316	MOV B, A
8234	7D	317	MOV A, L
8235	B8	318	CMF B
8236	CA3D82	319	JZ CN
8239	2C	320	INR L
823A	C34082	321	JMP CN1
823D	2A0140	322	CN: LHLD 4001H
8240	221B40	323	CN1: SHLD 401BH
8243	2A0C40	324	LHLD 400CH
8246	2B	325	DCX H
8247	220C40	326	SHLD 400CH
824A	E1	327	POP H
824B	D1	328	POP D
824C	C1	329	POP B

LOC	OBJ	LINE	SOURCE STATEMENT
824D	F1	330	POP PSW
824E	3E00	331	MVI A, 00H
8250	D3C2	332	OUT OC2H
8252	FB	333	EI
8253	C9	334	RET
8254	00	335	NOP

DISPLAYS THE FAILURE OF PULSE

8255	78	336	FFAI: MOV A, B
8256	2F	337	CMA
8257	A1	338	ANA C
8258	57	339	MOV D, A
8259	015044	340	LXI B, 4450H
825C	CD3804	341	CALL PNTMS
825F	C38982	342	JMP FDTR
8262	00	343	NOP

DISPLAYS MISFIRE AND SING COMMUATATION FAILURE

8263	78	344	TFCF: MOV A, B
8264	FE02	345	CPI 02
8266	FA7582	346	JM MFIR
8269	210044	347	LXI H, 4400H
826C	6A	348	MOV L, D
826D	DBC2	349	IN OC2H
826F	E607	350	ANI 07H
8271	BE	351	CMF M
8272	CA7F82	352	JZ SCF
8275	016044	353	MFIR: LXI B, 4460H
8278	CD3804	354	CALL PNTMS
827B	C38982	355	JMP FDTR
827E	00	356	NOP
827F	017044	357	SCF: LXI B, 4470H
8282	CD3804	358	CALL PNTMS
8285	C38982	359	JMP FDTR
8288	00	360	NOP
8289	7A	361	FDTR: MOV A, D
828A	0636	362	MVI B, 036H
828C	0F	363	REPR: RRC
828D	DA9482	364	JC FND
8290	05	365	DCR B
8291	C38C82	366	JMP REPR

THE FOLLOWING FINDS THE THYRISTOR INVOLVED

8294	78	367	FND: MOV A, B
8295	CD6702	368	CALL FRINT
8298	CDB702	369	CALL CRLF
829B	C1	370	POP B
829C	CF	371	RST 1

EXTERNAL SYMBOLS

USER SYMBOLS

BIHEX	A 03BD	CBASE	A 8000	CN	A 823D	CNI	A 8240
DECPU	A 80BE	DEVOL	A 8087	DIA	A 81BE	DIDA	A 80E3

DIFT	A 81A6	DIHE	A 8179	DIND	A 8196	DSP	A 804C
FDTR	A 8289	FFAI	A 8255	FND	A 8294	LP1	A 81FB
PRINT	A 0267	RCP1	A 802B	RCPY	A 8007	RDE	A 80C3
REPR	A 828C	ROT	A 817D	RSP	A 807E	SCF	A 827F
VOL6	A 80AB						

CP1	A 801D	CPY	A 8000	CRLF	A 02B7
DIF	A 811A	DIFO	A 814B	DIF6	A 815F

ECP1	A 8041	EDIH	A 8191	FAU	A 81D8
LP2	A 8209	MFIR	A 8275	FNTMS	A 0438
RDE1	A 80D8	RDIA	A 81C4	RDCP	A 805C
SPDI	A 807C	TFCF	A 8263	TWOSP	A 02C4

